PERFORMANCE STUDY OF HVDC LINK WITH GTO INVERTER

by

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SRI NIWAS SINGH

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CERTIFICATE

This is to certify that this work entitled "PERFORMANCE STUDY OF HVDC LINK WITH GTO INVERTER " by Sri Niwas Singh has been carried out under our supervision and this work has not been submitted elsewhere for the award of a degree.

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Sri Niwas Singh

Sri Niwas Singh

LIST OF FIGURES

ABSTRACT

In this thesis, a GTO converter having six GTOs is considered for state space model development. This model has been developed, based on the graph theoretic approach which is conceptually simpler and leads to efficient formulation of the converter equations corresponding to all possible modes of operation. The state equations are derived using network cutset matrix which can be modified conveniently depending upon the converter conduction pattern. The results of steady state test simulation are presented for both modes of the GTO converter operation (rectifier / inverter) to illustrate the validity of model and capability of program developed.

The performance of the HVDC link with GTO inverter has been studied under both normal and abnormal conditions.The system fault studies are change in current reference and ac voltage dips at both end of the converter. The harmonic analysis are performed for both normal and abnormal conditions.

CHAPTER 1

INTRODUCTION

High voltage direct current (HVDC) transmission has become a viable alternative to alternating current transmission for bulk power exchange. The earlier HVDC installations used mercury arc valves for power conversion. After the advent of thyristor, the most of the HVDC installations employ thyristor valves in converters which operate under natural (line) commutation. The problems of reactive power requirement and harmonic generation in case of line commuted converters are well documented in the literature [1]. These problems assume greater significance in case of the dc transmission and particularly when the power transmission capability of the line is being continuously upgraded. Traditionally, the harmonics generated by converters (rectifier/invereter) are not allowed to enter the associated ac system by using tuned filters at the converter ac bus. The filters can effectively shunt only the characteristic (6n+1 ,n=1,2,....) harmonics while the uncharacteristic harmonics may still enter the ac system and may cause harmonic instability [2]. The reactive power requirement of converters which may be typically 50% of the real power under normal operation, is met to a certain extent by installing shunt capacitors. Also, the harmonic filter which produces reactive power at fundamental frequency, provides some reactive power support. To circumvent the

problem of reactive power requirement and harmonic generation, the use of forced commutation in thyristor converters has been envisaged particularly with reference to inverter operation [3]. Pulse Width Modulated (PWM) ac-dc thyristor converters have been suggested to overcome the drawbacks of reactive power and hormonic generation. Although, it improves power factor and reduces harmonics, but the requirement of large number of auxiliary power devices and LC elements for the purpose of forced commutation of thyristors make these converters heavy, expensive and less reliable. Recently the availability of Gate Turn Off (GTO) thyristors with improved reliability and high ratings have made them attractive to be used in PWM ac-dc converters. With this, better power factor at ac side, less distortion of the line current and reduced ripple in dc current are achieved. As a GTO requires no commutation arrangement in the power circuit and can be turned off by a negative gate signal, its use as a power device, in place of a thyristor with forced commutation arrangement, greatly simplifies the converter configuration.The application of gate turn off(GTO) thyristor in low power circuits has been reported in literature [4]. It may be interesting to examine its application in HVDC converters (particularly inverters)using pulse width modulation (PWM) scheme.

1.1 GTO CONVERTER WITH PWM

In view of the advantages, a number of PWM schemes for ac-dc converters have been listed [4,5]. All these schemes have their own merits and demerits as regards to performance on source

and load side.The comparative study of various PWM schemes have been made for three phase PWM ac-dc converter employing GTO thyristors connected to an active load [4]. The basis for comparison is the source side performance such as power factor, distortion of line current, percentage of lower order harmonics in line current with fundamental component and the load side performance such as ripple content in the output current. Mainly five different types of PWM schemes, viz:(i)Equal (ii) Triangular (iii) Stepped (iv) Sinusoidal and (v) Inverted sinusoidal are in vogue. Among these schemes, Equal Pulse Width Modulation (EPWM) scheme has been found to offer the best overall performance [4].

The various pulse width modulation schemes can be used with converter configuration which employ either all 6 GTOs or 3 GTOs and 3 thyristors. While the latter offers economy in cost as GTO is a very expensive device compared to a converter grade thyristor but it requires large number of switching operations per cycle thus increasing the switching losses. Furthermore in the latter configuration firing pulses are to be reset for a different gating sequence whenever the operation has to be changed from rectification to inversion mode or vice-versa. Since turn on and turn off of a GTO is under an external control, the gating patterns (which turn on & turn off a GTO) could either be symmetrical or unsymmetrical [4]. In view of the above description, the six GTOs converter circuit employing symmetrical gating sequence based on equal pulse width modulation scheme, has been considered in this thesis for various investigations.

1.2 OBJECTIVES OF THE THESIS

The primary objectives of this thesis are :

(i) to examine the feasibility of using GTO converters as inverter in HVDC transmission system. This investigation is carried out through detailed dynamic digital simulation of a two terminal HVDC link.

(ii) development of a suitable mathematical model of a GTO converter for the purpose of simulation.

1.3 OUTLINE OF THE THESIS

In chapter 2 , a brief review of the literature on the PWM converters and various simulation techniques is presented.

The detailed modelling of GTO converter is given in chapter 3. This chapter also includes firing schemes (i.e. symmetrical and unsymmetrical) and effects of source inductance. The state space model is developed for the GTO converter with active load and RC transient suppressor circuit. Using the concept of graph theory, a generalised set of differential equations is formulated. The results of simulation are also presented in this chapter for both rectifier and inverter operation.

Chapter 4 describes the modelling of the constituents of an HVDC system in brief. Emphasis is laid on interfacing of GTO inverter and its controls in place of thyristor inverter using appropriate interfacing variables. The model developed in chapter 3 for GTO converter is used to study the performance of HVDC link. A computer program is developed to demonstrate the feasibility of GTO inverter in HVDC link. The disturbances considered, to stud

the dynamic behaviour, the change in current reference setting and ac voltage dips at both rectifier and inverter terminals.

The conclusions and future scope of the work are given in the chapter 5.

CHAPTER 2

LITERATURE REVIEW ON GTO CONVERTERS AND RELATED TOPICS

A brief review on pulse width modulated GTO converters and simulation techniques are given in this chapter.

2.1 PULSE WIDTH MODULATION

Line commuted converters are widely used in power industries because they are simple and reliable. However, these converters deteriorate the power factor at the source specially at large phase angles and they also introduce lower order harmonics in the source current which can be filtered out only by a large size LC filters. The HVDC transmission, using line commuted thyristor converter suffers from the problems of lagging reactive power requirement at the inverter and the commutation failure under abnormal conditions. Pulse Width Modulated (PWM) ac-dc thyristor converters have been suggested to overcome these drawbacks. Although, they improve power factor and reduce hormonics but require large number of auxiliary power devices which make the converter heavy, expensive and less reliable. Availability of high power GTO thyristor which can be turned on and off at desired instant, offers a suitable alternative. The PWM techniques employing forced commutation can make the fundamental power factor unity or even leading in the entire control range of the output voltage. But few voltage pulses per cycle introduce more ripples in the

output current and lower order harmonics in the source current. The width of output voltage pulses is continuously modulated throughout the ac cycle according to the modulation of a modulating signal and the PWM scheme is named after the corresponding modulating signal. A number of PWM schemes such as Equal Pulse-Width modulation (EPWM),Trangular Pulse-Width Modulation (TPWM),Stepped Pulse-Width Modulation (STPWM),Sinusiodal Pulse-Width Modulation (SPWM) and Inverted Pulse-Width Modulation (ISPWM) are reported in the literature [4].

2.2 COMPERATIVE PERFORMANCE OF VARIOUS PWM SCHEMES

The detailed comparative study of source and load side performances of a three phase PWM ac-dc converter employing different PWM schemes is given by Khan [4]. The effect of varying the number of output voltage pulses is also given. The switching instants are determined by comparing a trangular carrier signal Vca with a modulating signal Vm as shown in Figure (2.1). The source is connected to the load for the duration when Vm>Vca. The frequency of carrier signal depends on the number of pulses(P) required in one cycle of ac source. The output voltage can be varied by varying the peak value, Vmm of the modulating signal with respect to the peak value, Vcam of carrier signal. The ratio Vmm/Vcam is termed as modulation index (m). The expression for different modulating signals and the corresponding firing angles (α's) and extinction angles (β's) for Kth pulse can be given as follows [4]

$$Vca=\pm Vcam[(P/\pi)*(wt)-(2K-1)]$$

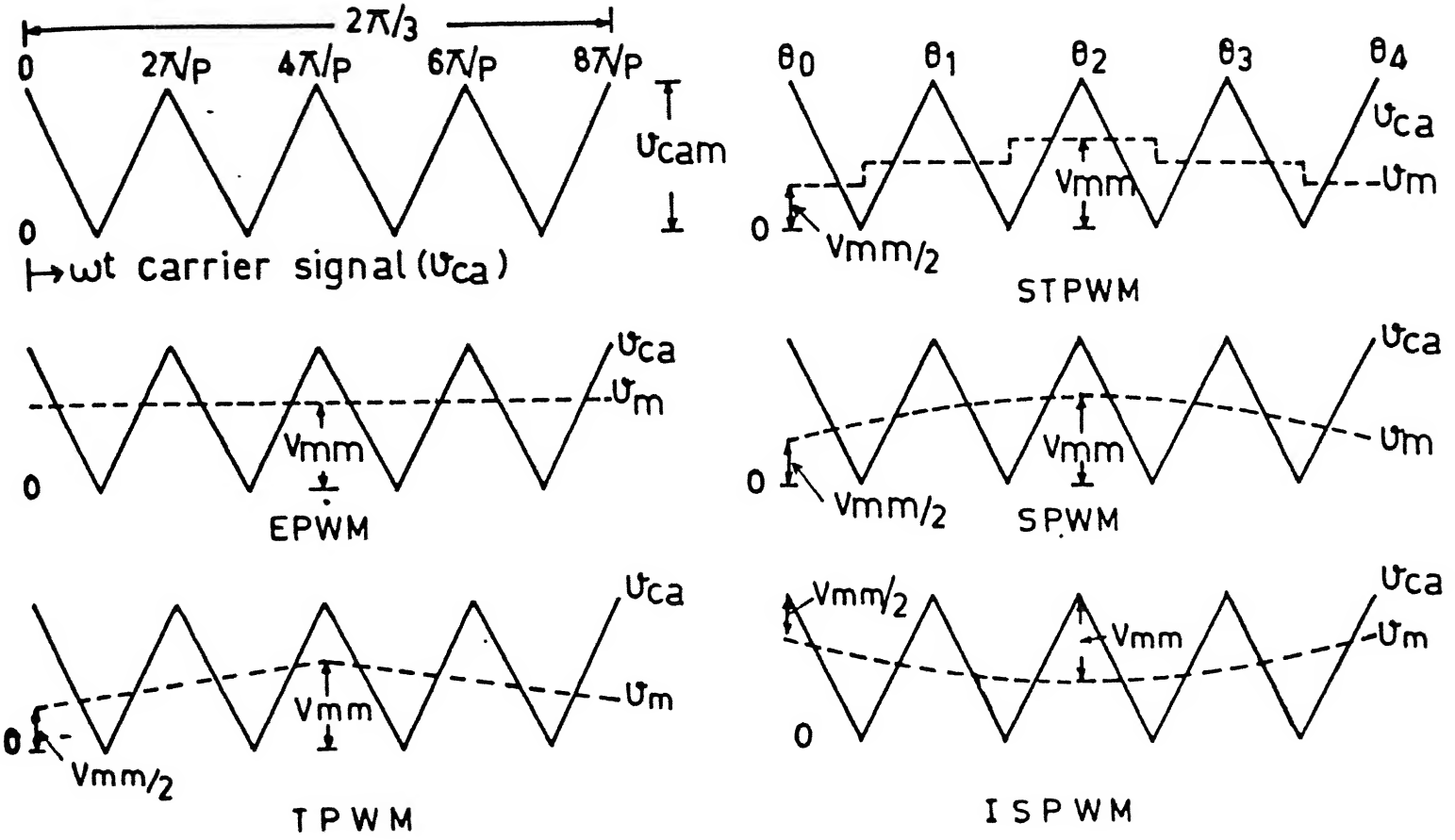


FIG.2.1. DIFFERENT MODULATION SCHEMES

Where + stands for positive slope and - stands for negative slope. The expression for firing and extinction angles for different modulation schemes are given in Table 2.1. It is reported in [4] that EPWM is superior to the other PWM schemes because of linearity between dc voltage ratio (γ) and modulation index (m) which is advantageous when the converter is used in a closed loop schemes. It is also reported that EPWM scheme results in least current ripples among various modulating schemes both in rectification and inversion operations. EPWM has only nP+1 and nP-1 source current harmonics. EPWM with 12 pulses per cycle is used in this thesis.

2.3 GATE TURN-OFF THYRISTOR (GTO)

GTOs were offered at the start of sixties with higher voltage capability but lower current capability. But since last few years they are available with ratings as high as 4.5 kV,3000 Amp. [6]. GTO thyristor is a silicon semiconductor power switch similar to an ordinary thyristor, but with a difference that it can be turned off (as well as on) by appropriate pulse at the gate terminal. Unlike an ordinary thyristor, which needs a higher power bulky circuit for turn off, GTOs can be turned off from a low power electronic circuit. As may be expected , GTO thyristor brings with its some drawbacks as well as advantages. Since turn off time of GTO thyristors is low, therefore the rate of change of anode current is very high. Unless the stray inductance is kept to a minimum, an excessive voltage will be developed across the inductance. The layout of snubber circuit requires special circuit to minimise stray

Table 2.1 : Expressions for different modulating signals and corresponding firing/extinction angles for Kth pulse.

	Modulating signal v_m	Firing angle α_K	Extinction angle β_K
EPWM	V_{mm}	$\frac{\pi}{P}(2K-1-m)$	$\frac{\pi}{P}(2K-1+m)$
TPWM	$\frac{V_{mm}}{2}(1+\frac{3}{\pi}\omega t)$ for positive slope $\frac{3V_{mm}}{2}(1-\frac{1}{\pi}\omega t)$ for negative slope	$\pi\frac{2(2K-1)-m}{3m+2P}$	$\pi\frac{2(2K-1)+m}{2P-3m}$
STPWM	$V_{mm}\sin(\theta_i+\pi/6)$ where $i = K-1$ for α and $i = K$ for β	$\frac{\pi}{P}[2K-1-m\sin\{\frac{2\pi}{P}(K-1)+\pi/6\}]$	$\frac{\pi}{P}[2K-1+m\sin(\frac{2\pi}{P}K+\pi/6)]$
SPWM	$V_{mm}\sin(\omega t+\pi/6)$	$m\sin(\alpha+\pi/6)+\frac{P}{\pi}\alpha$ $-2K+1 = 0$	$m\sin(\beta+\pi/6)-\frac{P}{\pi}\beta$ $+2K-1 = 0$
ISPWM	$V_{cam}[1-m\sin(\omega t+\pi/6)]$	$m\sin(\alpha+\pi/6)-\frac{P}{\pi}\alpha$ $+2K-2 = 0$	$m\sin(\beta+\pi/6)+\frac{P}{\pi}\beta$ $-2K = 0$

nductances [7,8,9]. There are two basic types of GTO hyristors, the anode shorted emitter and the gold diffused evice. Due to some advantages, the gold diffused devices are refered [8]. Both GTO thyristors and conventional hyristors are latching devices. Once the anode current reaches o a certain latch-on value , the device will automatically go nto a full conduction state. Only difference is that onventional thyristors can be brought back to the blocking tate only by reducing the forward anode current below the olding current and GTO thyristor can be brought back to the locking state by applying a negative gate signal [8,10].

2.4 PWM AC-DC GTO CONVERTERS

Basically, there are two types of PWM ac-dc converters as given below.

2.4.1 Three GTOs and Three Thyristors PWM AC-DC Converter

Three GTOs and three SCR thyristors converter configuration is proposed by INABA et al [11] which is given in Figure (2.2). Since GTOs are more costly than the ordinary thyristors, this converter has lower cost than the converter using six GTOs. The main problem is that a modification of gating sequence will be required to operate the converter in inversion mode. Overlapping between the conduction period of the outgoing and incoming GTOs is also provided to ensure the continuity of load current.

2.4.2 Six GTOs PWM AC-DC Converter

The advantage of using six GTOs is that one can use optimal PWM control schemes, where particular harmonics can be

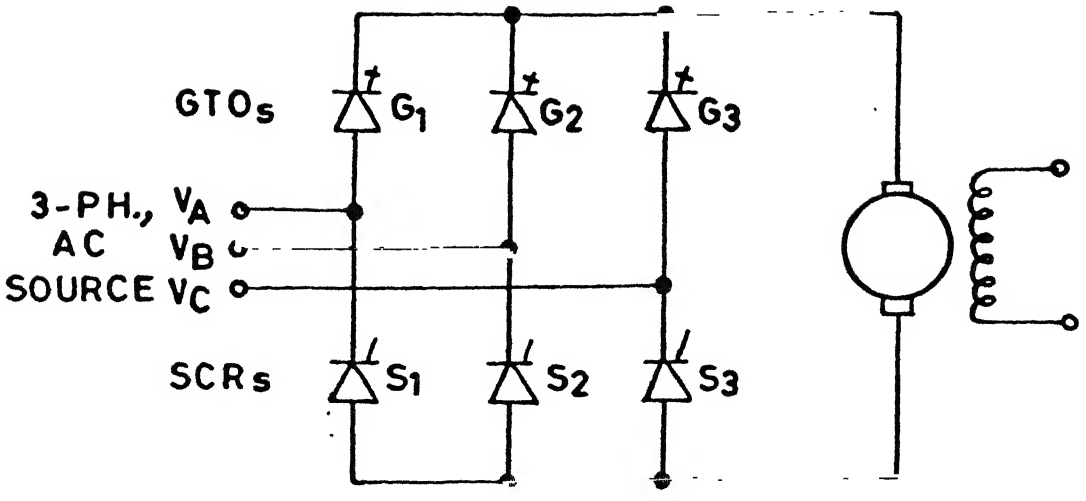


FIG.2.2 CONVERTER CIRCUIT GIVEN BY INABA et al.

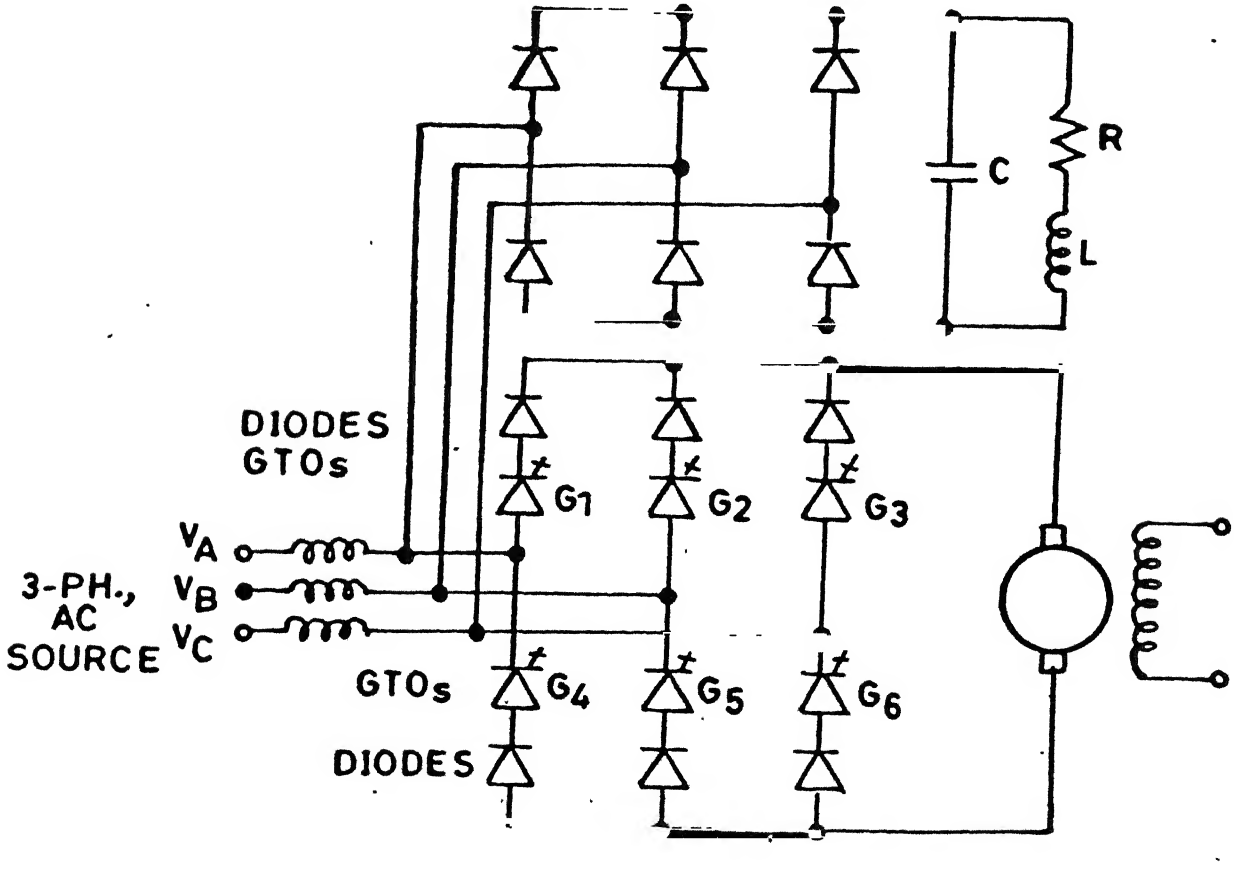


FIG.2.3. CONVERTER GIVEN BY KATAOKA et al.

inimized, but it increases the switching times leading to ncrease in switching losses. There is no requirement of odification of gating sequence to shift operation from ectification mode to inversion mode or vice-versa. Because he GTO is expensive compared to thyristor,the six GTOs PWM c-dc converters are more costly than three GTOs and three hyristors convertors. The six GTOs configuration is given by (atakoa et al [12] which is given in Figure (2.3).

2.5 SUPPRESSION OF SWITCHING SPIKES

When the source current is forced to zero, the source inductance produces voltage spikes which must be kept to the acceptable level. An RC filter is often connected on ac side for this purpose. This leads to substantial wastage of power, consequently PWM converters have lower efficiency. Viriya et al [13] have suggested an alternative circuit for suppresion of the voltage spikes, which improves the converter efficiency significantly and is given in Figure (2.4). An auxiliary circuit capacitor is used to clamp the commutating voltage spikes at the desired level. The reactive energy stored in the source reactance, at the time of commutation of each GTO in the main circuit is passed through to the capacitor in the auxiliary circuit. The energy stored in the capacitor is then discarged in pulses to the dc load during on state of the GTOs in the auxiliary circuit. By this method the snubber capacitor becomes smaller or even unnecessary.

2.6 SIMULATION TECHNIQUES

For study purpose, there are two type of models

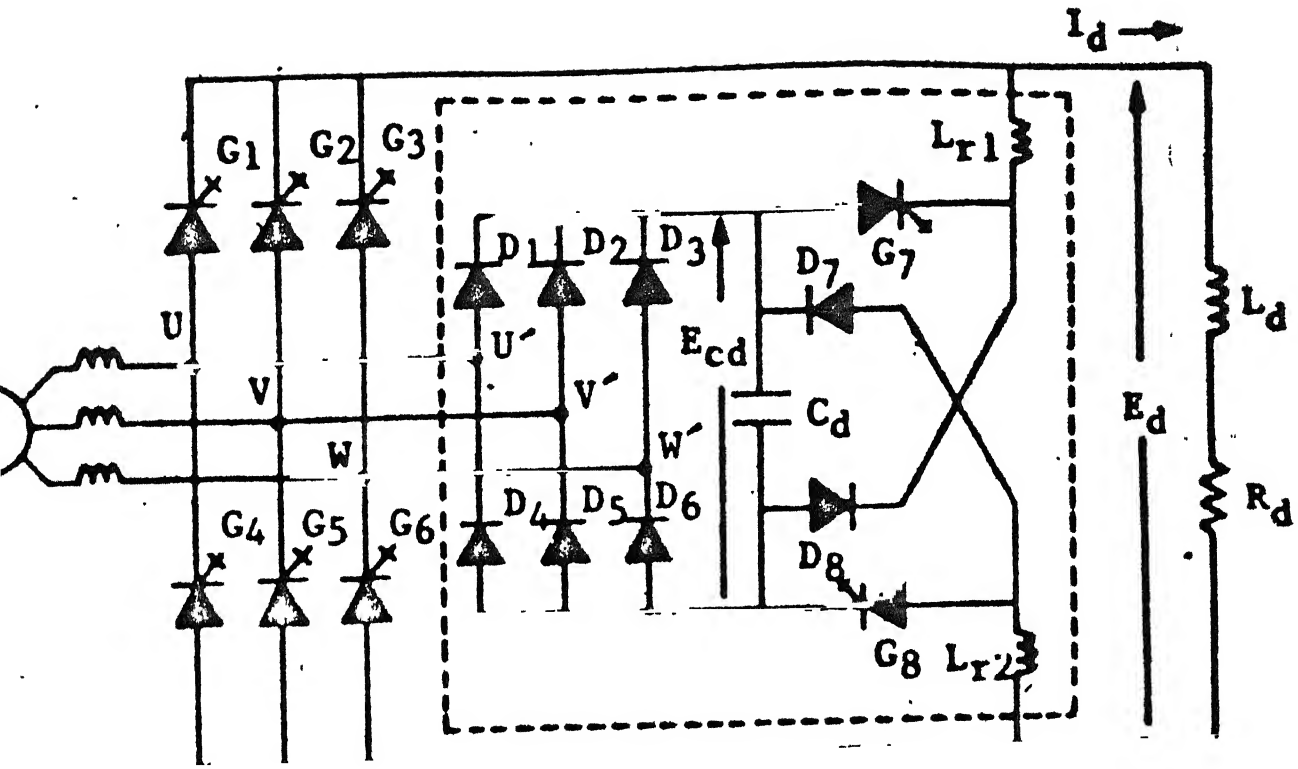


FIG. 2.4 SWITCHING SPIKES SUPPRESSION CIRCUIT WITH PWM GTO CONVERTER

namely, physical and analytical. Physical model has advantage of experimentation but it is less flexible. The mathematical description of the system characteristic in the form of algebraic and differential equations has the advantages such as flexibility for analysing with different input-output parameters, usefulness for studying various system alternatives etc. Although some assumptions have to be made for analytical model. There are four basic simulation techniques which have been employed for the study of power semicoductor circuit [5].

(1) Digital Simulation

(2) Analog Simulation

(3) Breadboard Simulation

(4) Parity Simulation

2.7 DIGITAL SIMULATION

For digital simulation, the system under study is characterised by a mathematical model. The dynamics of the system can be discribed in the general state space form as

$$\dot{\underline{X}}=[A]\underline{X}+[B]\underline{U} \qquad (2.1)$$

$$\underline{Y}=[C]\underline{X}+[D]\underline{U} \qquad (2.2)$$

where $\underline{X}$ is the set of the system state variables, $\underline{U}$ is the vector of forcing functions, $\underline{Y}$ is the set of output variables of interest. The matrices [A],[B],[C] and [D] are system matrices and depend upon physical characteristics and parameters of the system. The state equation (2.1) is solved using numerical integration and set of output variables are calculated at each time step by equation (2.2). The varying circuit configuration

leads to the time dependent nature of the system matrices and thus formulation of the state and output equations are not straight forward. The dynamic representation of the power circuits has been reported in the literature [14] based on

(a) constant topology approach

(b) varying topology approach

2.7.1. Constant Topology Approach

In constant topology approach the network structure is made time invariant for all modes of operation by suitable representations of the devices. The switching devices are represented by a low resistance when conducting and by high resistance when not conducting. This model runs the risk of numerical instability because of widely varying time constants if the step size of integration is not suitably selected. The problem relating to varying time constant is solved with a new model for switching devices. In the nonconducting state of the switching device the reverse resistance is arranged in series with an appropriate value of fictitious inductance so that this time constant is larger than the real time constant in the circuit. The switching devices may be represented by a combination of forward and backward resistance to that structure of the signal flow graph is independent of the mode of operation. Another way to represent the switching devices is to adjust voltage source.

2.7.2.Varying Topology Approach

In this approach the switching devices are so modelled that the network exhibits a time varying structure. The

equations are formulated from the reduced network structure for the particular mode of operation with time varying structure. Spurious time constants are not introduced in mathematical model and also the order of the system matrices is minimum for a particular mode of operation. Various models reported in the literature represent the switching device during off state by an infinite impedance (i.e. zero current through device) and during on state either by zero impedance (i.e. zero voltage drop across deivce) or by small resistance. Sachchidanand et al [15] have represented the converter based on the graph theoratic framework for the detailed dynamic simulation of a three phase bridge converter. This approach not only formulates the system state equations efficiently for all possible modes but also gives the expression of dependent variables. This enables to analyse the converter during both normal and abnormal modes of operation. The most attractive feature of analog simulation technique is the inherent speed of an analog computer which makes the parametric system studies practical. The major drawback is in topological restructuring of the computer. Availability of high speed digital computers, the use of analog computers became obselete. The appealing advantage of bread board simulation turns out to be that it uses the system description familiar to the engineer i.e. schematic diagram. But this technique is rather inflexible. The parity simulation is also not without shortcomings. The chief among them are perhaps, the dedicated natural synthetic components and the realization are also not simple[14].

CHAPTER 3

MODELLING OF GTO CONVERTER

3.1 INTRODUCTION

Forced commutation circuitry provided with thyristors increases the complexity of the convereter configuration. In recent times, GTOs are finding application where earlier forced commutating thyristors were being used. This results into simplified converter configuration due to the absence of commutating elements in the power circuitry.

In this chapter a three phase six GTOs converter system representation, based on graph theoretic analysis is described.The approach is conceptually simpler and leads to efficient formulation of the converter equations corresponding to all possible modes of operation. The state equations are derived using network cutset matrix which can be modified conveniently depending upon converter conduction patterns. The topological analysis leads not only to the system equations but also to the expression of dependent variables such as voltage across GTO valves, etc.

The results of steady state test simulations are presented for both modes of the GTO converter operation (rectifier/ inverter) to illustrate the validity of converter model and the capability of computer program developed.

3.2 CONVERTER SYSTEM

A converter system employing six GTOs is shown in Figure (3.1).This includes the leakage impedance of converter transformer (R_s,L_s) and the dc smoothing reactor (R_d,L_d). The effect of the ac system on the converter is represented by the source voltages (e_1,e_2,e_3). The system also includes a transient suppressor circuit (R,C) connected across the supply. In parallel to each GTO , a snubber circuit is connected comprising of a series RC circuit with a diode in parallel. In series with each GTO, a diode with R_d–C_d combination in parallel, is provided to give the reverse voltage blocking capability to the GTO. The dc network is also represented as a voltage source (V_d) at the converter terminals.

If the objective of the digital simulation is to investigate the control system response in the frequency range upto 1 kHz, the converter circuit of Figure (3.1) can be simplified as follows:

1. The snubber circuit can be neglected, since the high frequency switching transients are not of interest.

2. The diodes and R_d–C_d combination in series with GTO can be ignored as GTO is assumed to have high reverse voltage capability.

Based on these assumptions, the simplified converter system configuration is shown in Figure (3.2).

3.2.1 Firing Scheme

The output of GTO converter can be varied continuously using pulse width control. Pulse width is controlled between

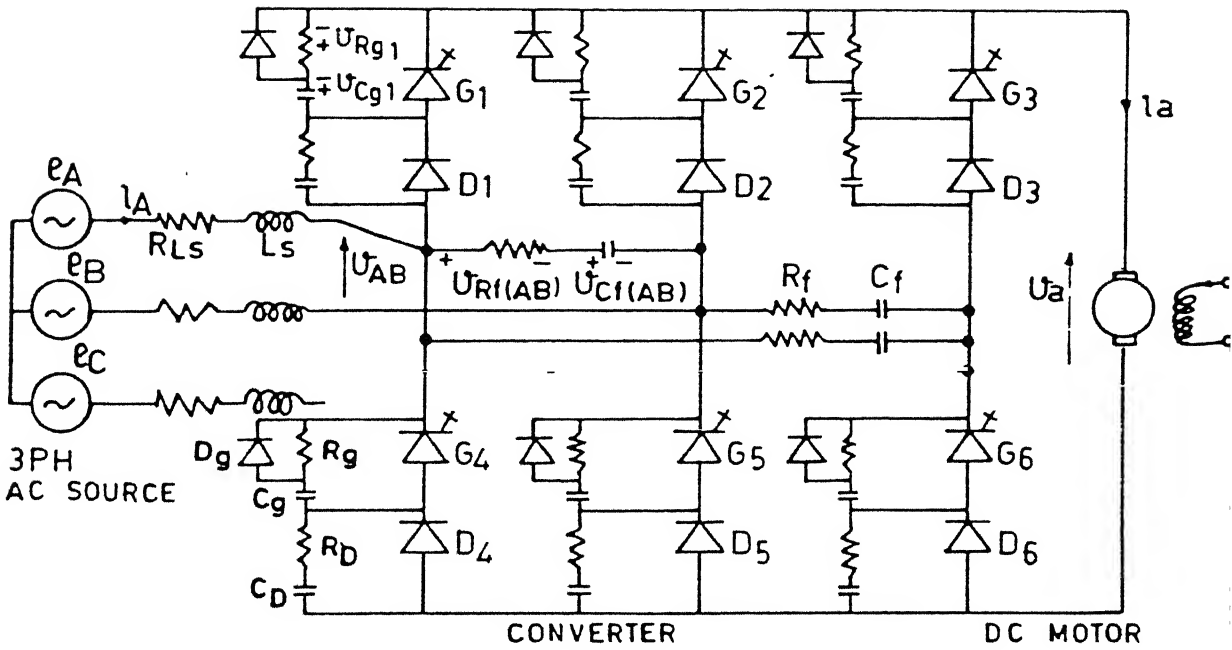


FIG. 3.1 COMPLETE CIRCUIT DIAGRAM OF THE PROPOSED CONVERTER SYSTEM.

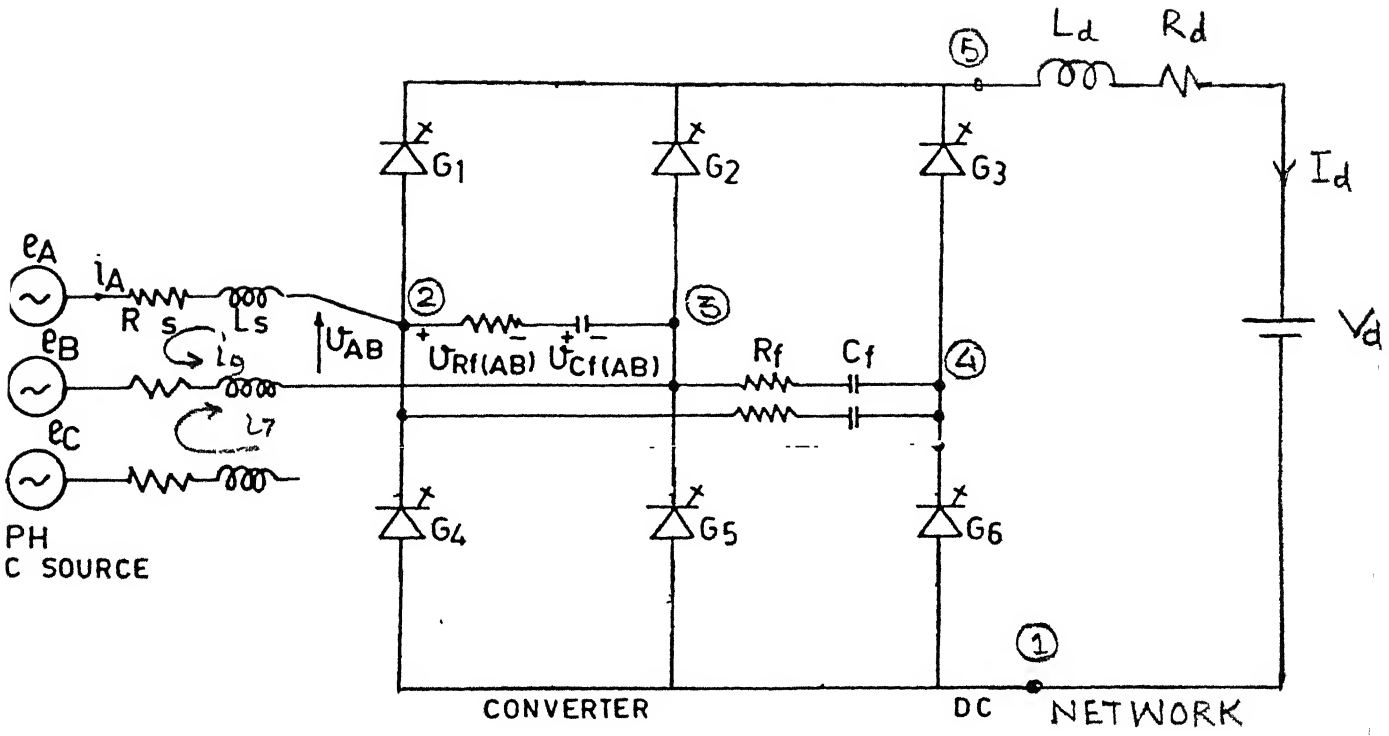


FIG. 3.2 SIMPLIFIED CONVERTER SYSTEM CONFIGURATION

maximum and minimum values, keeping its position fixed. Among various PWM schemes the Equal Pulse Width Modulation (EPWM) is used due to certain advantages. EPWM firing scheme can be implimented using two types of gating patterns.

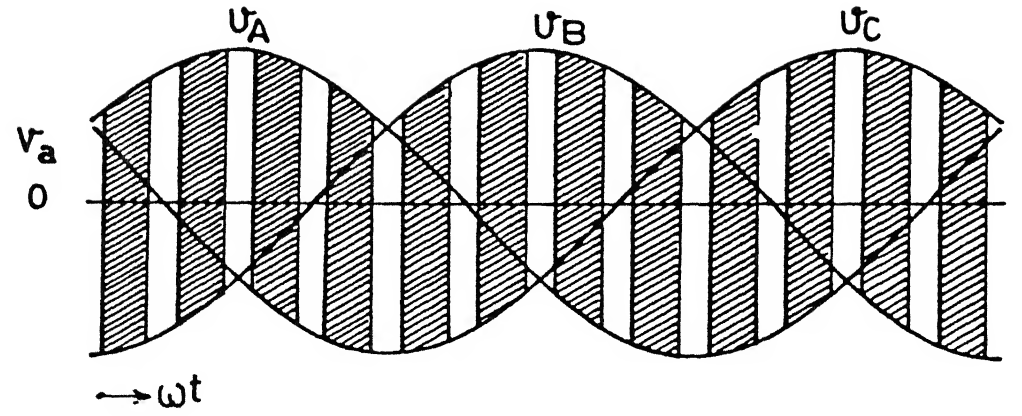
1. Symmetrical and

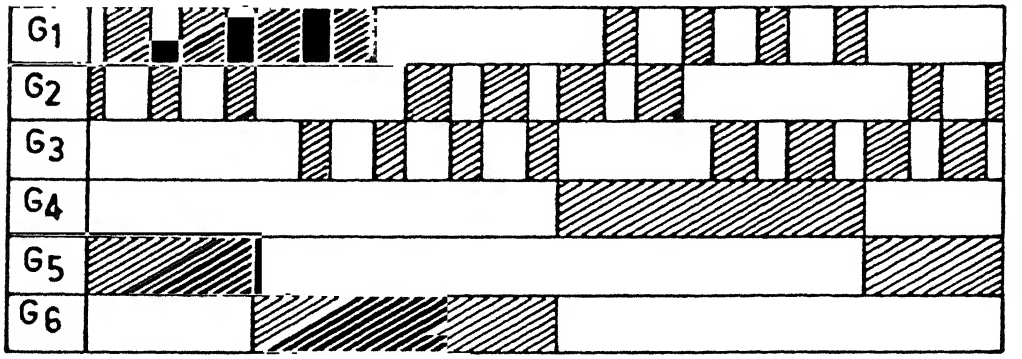
2. Unsymmetrical

The gating patterns are shown in Figure (3.3). In case of unsymmetrical gating , GTOs in upper valve group (G_1,G_3,G_5) are gated by more than one gate pulse while those in the lower valve group (G_2,G_4,G_6) are gated only once during a cycle. In symmetrical gating the switching numbers are same for all the GTOs. Comparing both these gating patterns, it may be observed from Figure (3.3) that number of switchings per ac cycle are 27 for unsymmetrical and 24 for symmetrical gating. Therefore, symmetrical gating results in less switching loss which is uniformly distributed among all the GTOs. To avoid any switching transient, there should not be any gap between OFF & ON gate pulse applied to outgoing and incoming GTOs.

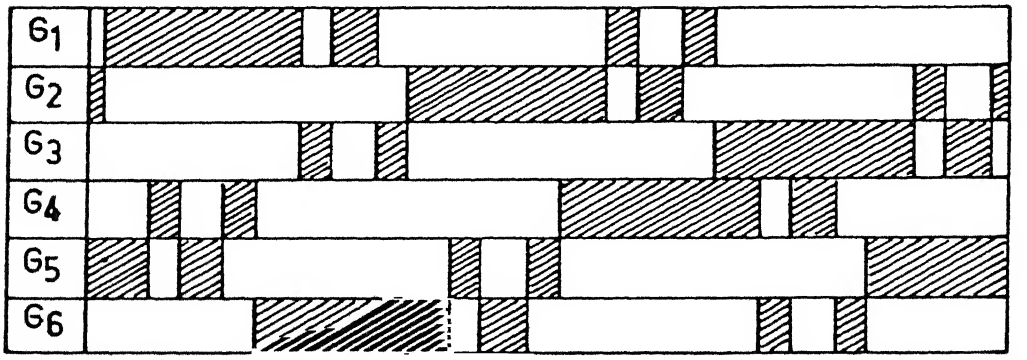
3.2.2 Effect of Source Inductance

In the presence of source inductance, an over-voltage appears across the snubber capacitance when current is interrupted by a GTO while turning off. The over-voltage depends on the value of source inductance and the magnitude of current interrupted. Increasing the size of snubber capacitor in order to suppress the over-voltage may not be appropriate as it would also increase the





(a) UNSYMMETRICAL GATING



(b) SYMMETRICAL GATING

FIG. 3.3. GATING PATTERNS

losses in the snubber circuit . A capacitor C is used across the source terminals to take care of the transients due to source inductance as shown in Figure (3.1). The value of C should not be very high as it would load the source permanently. A resistor R is provided for damping.

The presence of source inductance also causes reduction in the average output voltage of the converter. Assuming that G_1 is turned off and G_3 is turned on at an instant (refer Figure 3.2). The current in phase B (i_b) starts increasing from zero and would assume the value I_d after some time. Since this current cannot increase instanteneously and I_d remains constant, a current i_t ($=I_d-i_b$) must be supplied by voltage absorbing circuit until i_b equals I_d. During this process a voltage $L_s.(di_b)/dt$ appears across inductance L_s.

The average output voltage (E_d) of the converter before the smoothing reactor can be calculated considering voltage drops due to the transformer resistance, inductance and switching devices as:

$$E_d = E_0 - \left(\frac{3P}{\pi}\omega L_s + \lambda R_s\right) I_d - V_T \qquad (3.1)$$

Where E_0 is the average output voltage when there is no drop. V_T is drop across the switching devices under conduction and λ is a constant. P denotes the number of pulses per ac cycle. The details of equation (3.1) are given in Appendix I. If R_s and V_T are assumed to be zero, the equation (3.1) can be written as:

$$E_d = E_0 - \left(\frac{3P}{\pi}\right)\omega L_s I_d \qquad (3.2)$$

A similar equation can be obtained for thyristor converters [1] as:

$$E_d = E_0 - (3/\pi)\omega L_s I_d \qquad (3.3)$$

It is evident from equation (3.2) that the voltage drop is dependent on pulse number in addition to the transformer leakage reactance and dc current . Hence, the value of P shuold be judiciously chosen.

3.3 MODEL FORMULATION

The graph of Figure (3.2) is shown in Figure (3.4). This has 5 nodes and 12 elements. Elements 1 to 6 correspond to GTOs (G_1 to G_6). The elements 7 and 9 are equivalent representation of the ac system feeding the converter. Element 8 represents the dc network which includes dc transmission line. Elements 10 to 12 represent the RC transient suppressor circuit. In general, the choice of elements considered in the formulation of a tree is based on the following priorities [5].

1. Voltage Sources
2. Capacitive Elements
3. Resistive Elements
4. Inductive Elements
5. Current Sources

For the graph shown in Figure (3.4), 4 elements (branches) are required to constitute a tree which for any network

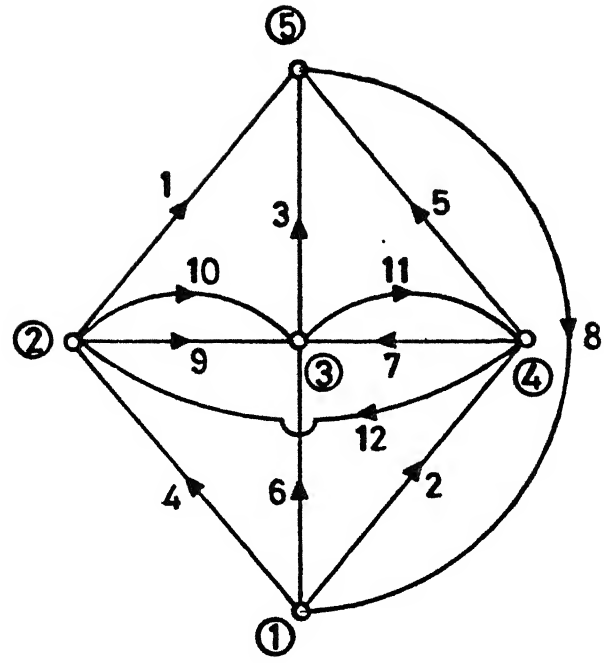


FIG.3.4 GRAPH OF THE SIMPLIFIED CONVERTER SYSTEM.

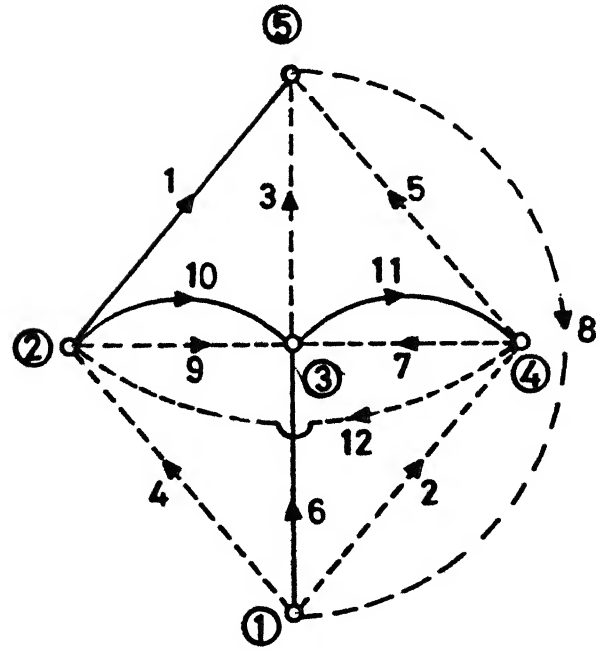


FIG.3.5 A TREE OF THE GRAPH

is not unique. The tree of the graph is chosen to include elements 10,11 and any two elements corresponding to the conducting GTOs , one from the upper valve group and other from the lower valve group. This is based on the assumption that the dc link current is continuous, hence one valve in the upper and lower valve group would always be conducting. Figure(3.5) shows the tree for the graph of Figure (3.4) with valves 6 and 1 assumed to be conducting. For any network, the branch and link variables are related by:

$$\underline{i}_B = -[B_L]\underline{i}_L \qquad (3.4)$$

$$\underline{v}_L = [B_L]^T \underline{v}_B \qquad (3.5)$$

where subscripts B and L of state vector refer to the branches and links respectively and matrix $[B_L]$ is the component of the fundamental cutset matrix. The matrices corresponding to the various trees which may be formed depending upon the converter conduction patterns, are given in the Appendix II. The branch variables can be further partitioned as:

$$\underline{v}_B = \begin{bmatrix} \underline{v}_{B1} \\ \underline{v}_{B2} \end{bmatrix} ; \quad \underline{i}_B = \begin{bmatrix} \underline{i}_{B1} \\ \underline{i}_{B2} \end{bmatrix} \qquad (3.6)$$

Where subscript 'B1' corresponds to elements 10 & 11and 'B2' corresponds to elements S_1 and S_2 i.e. conducting GTOs included in the tree. Similarly, the link variables can be partitioned as given below:

$$\underline{V}_L = \begin{bmatrix} \underline{V}_{L1} \\ \underline{V}_{L2} \\ \underline{V}_{L3} \\ \underline{V}_{L4} \end{bmatrix} \quad ; \quad \underline{i}_L = \begin{bmatrix} \underline{i}_{L1} \\ \underline{i}_{L2} \\ \underline{i}_{L3} \\ \underline{i}_{L4} \end{bmatrix} \qquad (3.7)$$

where subscript 'L_1' corresponds to elements 7,8 & 9

'L_2' corresponds to element 12

'L_3' corresponds to nonconducting GTOs &

'L_4' corresponds to conducting GTOs in link.

From the partitioning of the branch and link variables, the matrix $[B_L]$ can be written as:

$$[B_L] = \begin{array}{c} \\ B_1 \\ B_2 \end{array} \begin{array}{c} \begin{array}{cccc} L_1 & L_2 & L_3 & L_4 \end{array} \\ \left[\begin{array}{c|c|c|c} B_{L11} & B_{L12} & B_{L13} & B_{L14} \\ \hline B_{L21} & B_{L22} & B_{L23} & B_{L24} \end{array}\right] \end{array} \qquad (3.8)$$

Using equations (3.6) to (3.8), equations (3.4) & (3.5) can now be written as:

$$\underline{i}_{B1} = -[B_{L11}]\underline{i}_{L1} - [B_{L12}]\underline{i}_{L2} - [B_{L13}]\underline{i}_{L3} - [B_{L14}]\underline{i}_{L4} \qquad (3.9)$$

$$\underline{i}_{B2} = -[B_{L21}]\underline{i}_{L1} - [B_{L22}]\underline{i}_{L2} - [B_{L23}]\underline{i}_{L3} - [B_{L24}]\underline{i}_{L4} \qquad (3.10)$$

$$\underline{V}_{L1} = [B_{L11}]^T\underline{V}_{B1} + [B_{L21}]^T\underline{V}_{B2} \qquad (3.11)$$

$$\underline{V}_{L2} = [B_{L12}]^T\underline{V}_{B1} + [B_{L22}]^T\underline{V}_{B2} \qquad (3.12)$$

$$\underline{V}_{L3} = [B_{L13}]^T\underline{V}_{B1} + [B_{L23}]^T\underline{V}_{B2} \qquad (3.13)$$

$$\underline{V}_{L4} = [B_{L14}]^T\underline{V}_{B1} + [B_{L24}]^T\underline{V}_{B2} \qquad (3.14)$$

In order to simplify the model formulation, the following assumptions are made.

1. GTOs offer zero impedance when on and infinite impedance when off.

2. Capacitances used in transient suppressor circuit are lossless.

Based on the first assumption the following relations are evident.

$$\underline{V}_{B2}=0 \quad ; \quad \underline{V}_{L4}=0 \quad ; \quad \underline{i}_{L3}=0 \tag{3.15}$$

Since there is no interaction between the elements included in set B_2 and element 12 under different operating modes of converter ,matrix $[B_{L22}]$ is a null matrix.

Thus, using equation (3.15), equations (3.9) to (3.14) are simplified as :

$$\underline{i}_{B1}= -[B_{L11}]\underline{i}_{L1}-[B_{L12}]\underline{i}_{L2}-[B_{L14}]\underline{i}_{L4} \tag{3.16}$$

$$\underline{i}_{B2}= -[B_{L21}]\underline{i}_{L1}-[B_{L24}]\underline{i}_{L4} \tag{3.17}$$

$$\underline{V}_{L1}= [B_{L11}]^T\underline{V}_{B1} \tag{3.18}$$

$$\underline{V}_{L2}= [B_{L12}]^T\underline{V}_{B1} \tag{3.19}$$

$$\underline{V}_{L3}= [B_{L13}]^T\underline{V}_{B1} \tag{3.20}$$

$$\underline{0} = [B_{L14}]^T\underline{V}_{B1} \tag{3.21}$$

The constituent equation for elements 7,8 & 9 is given by,

$$\underline{V}_{L1}= [R_a]\underline{i}_{L1}+[\omega L_a]p\underline{i}_{L1}+\underline{e} \tag{3.22}$$

where

$$\underline{V}_{L1}=\left[V_7 \ , V_8 \ , V_9\right]^T \quad ; \quad \underline{i}_{L1}=\left[i_7 \ , i_8 \ , i_9\right]^T$$

Assuming the transformer resistance and leakage reactance to be equal in all the three phases.

$$[R_a] = \begin{bmatrix} 2R_s & 0 & R_s \\ 0 & R_d & 0 \\ R_s & 0 & 2R_s \end{bmatrix} \quad ; \quad [\omega L_a] = \begin{bmatrix} 2\omega L_s & 0 & \omega L_s \\ 0 & \omega L_d & 0 \\ \omega L_s & 0 & 2\omega L_s \end{bmatrix}$$

$$\underline{e} = \begin{bmatrix} e_3 - e_2 \\ V_d \\ e_1 - e_2 \end{bmatrix} \quad ; \quad p = \frac{d}{d(\omega t)} \quad ; \quad \omega = 2\pi f$$

Where e_1, e_2 and e_3 are the three phase ac supply voltages, V_d is voltage source representing dc network. R_d and L_d are smoothing resistance and inductance respectively. For branches 10 & 11, the basic equation is:

$$p\underline{V}_{B1} = [R_f] p\underline{i}_{B1} + [C'_f]\underline{i}_{B1} \qquad (3.24)$$

where

$$[R_f] = \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \quad ; \quad [C'_f] = \begin{bmatrix} \frac{1}{\omega C} & 0 \\ 0 & \frac{1}{\omega C} \end{bmatrix}$$

;R and C are transient suppressor circuit elements.

$$\underline{V}_{B1} = \begin{bmatrix} V_{10} \\ V_{11} \end{bmatrix} \quad ; \quad \underline{i}_{B1} = \begin{bmatrix} i_{10} \\ i_{11} \end{bmatrix}$$

Similarly for element 12, the following expression can be written.

$$p\underline{V}_{L2} = R.p\underline{i}_{L2} + C_f \underline{i}_{L2} \quad ; \quad C_f = 1/\omega C \qquad (3.25)$$

With suitable manipulations of equations (3.16) to (3.25), the following equation is obtained:

$$p\begin{bmatrix} \underline{i}_{L1} \\ \underline{i}_{L4} \\ \underline{V}_{B1} \end{bmatrix} = \begin{bmatrix} [K_1] & 0 & [K_2] \\ [K_{12}] & [K_{11}] & [K_{13}] \\ [-K_{15}] & [-K_{16}] & [-K_{17}] \end{bmatrix} \begin{bmatrix} \underline{i}_{L1} \\ \underline{i}_{L4} \\ \underline{V}_{B1} \end{bmatrix} + \begin{bmatrix} [K_3] \\ [K_{14}] \\ [-K_{18}] \end{bmatrix} \underline{e} \quad (3.26)$$

The detailed derivation of equation (3.26) is give in Appendix III.The formulation of state equation for two different modes of converter operation is illustrated using the generalised state equation (3.26).

CASE I

This case corresponds to the power mode operation of the converter in which say GTOs G_6 and G_1 are conducting. The submatrices for this mode of operation can be derived based on the cutset matrix formed for the tree with S_1=6 and S_2=1, as given below:

$$[B_{L11}]=\begin{bmatrix} 0 & 1 & 1 \\ -1 & 0 & 0 \end{bmatrix} ; [B_{L12}]=\begin{bmatrix} -1 \\ -1 \end{bmatrix} ; [B_{L13}]=\begin{bmatrix} 0 & -1 & -1 & -1 \\ 1 & 0 & 0 & -1 \end{bmatrix}$$

$$[B_{L21}]=\begin{bmatrix} 0 & -1 & 0 \\ 0 & -1 & 0 \end{bmatrix} ; [B_{L23}]=\begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix} ; [B_{L14}]=[B_{L24}]=[0]$$

$$[K_3]=-[\omega L_a]^{-1} =-\begin{bmatrix} \frac{2}{3\omega L_s} & 0 & \frac{-1}{3\omega L_s} \\ 0 & \frac{1}{\omega L_d} & 0 \\ \frac{-1}{3\omega L_s} & 0 & \frac{2}{3\omega L_s} \end{bmatrix}$$

$$[K_1] = -[\omega L_a]^{-1}[R_a] = -\begin{bmatrix} \frac{2}{3\omega L_s} & 0 & \frac{-1}{3\omega L_s} \\ 0 & \frac{1}{\omega L_d} & 0 \\ \frac{-1}{3\omega L_s} & 0 & \frac{2}{3\omega L_s} \end{bmatrix}\begin{bmatrix} 2R_s & 0 & R_s \\ 0 & R_d & 0 \\ R_s & 0 & 2R_s \end{bmatrix}$$

$$= \begin{bmatrix} \frac{-R_s}{\omega L_s} & 0 & 0 \\ 0 & \frac{-R_d}{\omega L_d} & 0 \\ 0 & 0 & \frac{-R_s}{\omega L_s} \end{bmatrix}$$

$$[K_2] = [\omega L_a]^{-1}[B_{L11}]^T$$

$$= \begin{bmatrix} \frac{2}{3\omega L_s} & 0 & \frac{-1}{3\omega L_s} \\ 0 & \frac{1}{\omega L_d} & 0 \\ \frac{-1}{3\omega L_s} & 0 & \frac{2}{3\omega L_s} \end{bmatrix}\begin{bmatrix} 0 & -1 \\ 1 & 0 \\ 1 & 0 \end{bmatrix} = \begin{bmatrix} \frac{-1}{3\omega L_s} & \frac{-2}{3\omega L_s} \\ \frac{1}{\omega L_d} & 0 \\ \frac{2}{3\omega L_s} & \frac{1}{3\omega L_s} \end{bmatrix}$$

$$[K_5] = -(1/(3R)).[B_{L12}]^T[R_f][B_{L11}]$$

$$= \begin{bmatrix} -(1/3) & (1/3) & (1/3) \end{bmatrix}$$

$[K_6]=0$; $[K_8]=0$

$$[K_7]=(1/(3\omega RC)).\begin{bmatrix} -1 & 1 & 1 \end{bmatrix}$$

$[K_{11}]=[0]$; $[K_{12}]=[0]$; $[K_{13}]=[0]$; $[K_{14}]=[0]$

$$[K_{19}]=R\left[[B_{L11}]+[B_{L12}][K_5]\right]$$

$$= R \begin{bmatrix} (1/3) & (2/3) & (2/3) \\ -(2/3) & -(1/3) & -(1/3) \end{bmatrix}$$

$[K_{20}]=[0]$; $[K_{22}]=[0]$; $[K_{16}]=[0]$

$$[K_{21}]=\begin{bmatrix} (1/3) & (2/3) & (2/3) \\ -(2/3) & -(1/3) & -(1/3) \end{bmatrix} \cdot \frac{1}{\omega C}$$

$[K_{15}]=[K_{19}][K_1]+[K_{20}][K_2]+[K_{21}]$

$$= \begin{bmatrix} \left(\frac{-R_s}{\omega L_s} + \frac{1}{\omega RC}\right) & \left(\frac{-2R_d}{\omega L_s} + \frac{2}{\omega RC}\right) & \left(\frac{-2R_s}{\omega L_s} + \frac{2}{\omega RC}\right) \\ \left(\frac{2R_s}{\omega L_s} - \frac{2}{\omega RC}\right) & \left(\frac{R_d}{\omega L_d} - \frac{1}{\omega RC}\right) & \left(\frac{R_s}{\omega L_s} - \frac{1}{\omega RC}\right) \end{bmatrix} .(R/3)$$

$$[K_{17}]= \begin{bmatrix} \left(\frac{2}{\omega L_d} + \frac{1}{\omega L_s}\right) & 0 \\ \frac{-1}{\omega L_d} & \frac{1}{\omega L_s} \end{bmatrix} .(R/3)$$

$$[K_{18}]= \begin{bmatrix} 0 & \frac{-2}{\omega L_d} & \frac{-1}{\omega L_s} \\ \frac{1}{\omega L_s} & \frac{1}{\omega L_d} & 0 \end{bmatrix} .(R/3)$$

The final set of equations can be obtained by putting above calculated submatrices in equation (3.26). The submatrices of different GTO conduction patterns can be calculated in the same manner.

CASE II

This case corresponds to the free wheel mode of converter operation in which $S_1 = 1$ and $S_2 = 4$. The submatrices for this mode of operation can be calculated as follows:

The value of submatrices $[K_1]$ and $[K_3]$ will be same as in case I.

$$[B_{L11}] = \begin{bmatrix} 0 & 0 & 1 \\ -1 & 0 & 0 \end{bmatrix} \; ; \; [B_{L12}] = \begin{bmatrix} -1 \\ -1 \end{bmatrix} \; ; \; [B_{L13}] = \begin{bmatrix} 1 & -1 & -1 & 1 \\ 1 & 0 & -1 & 0 \end{bmatrix}$$

$$[B_{L21}] = \begin{bmatrix} 0 & -1 & 0 \\ 0 & -1 & 0 \end{bmatrix} \; ; \; [B_{L23}] = \begin{bmatrix} 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 \end{bmatrix} \; ; \; [B_{L14}] = [B_{L24}] = [0]$$

$$[K_2] = [\omega L_a]^{-1} [B_{L11}]^T$$

$$= \begin{bmatrix} \frac{2}{3\omega L_s} & 0 & \frac{-1}{3\omega L_s} \\ 0 & \frac{1}{\omega L_d} & 0 \\ \frac{-1}{3\omega L_s} & 0 & \frac{2}{3\omega L_s} \end{bmatrix} \begin{bmatrix} 0 & -1 \\ 0 & 0 \\ 1 & 0 \end{bmatrix} = \begin{bmatrix} \frac{-1}{3\omega L_s} & \frac{-2}{3\omega L_s} \\ 0 & 0 \\ \frac{2}{3\omega L_s} & \frac{1}{3\omega L_s} \end{bmatrix}$$

$$[K_5] = -(1/(3R)).[B_{L12}]^T [R_f] [B_{L11}]$$

$$= \begin{bmatrix} -(1/3) & 0 & (1/3) \end{bmatrix}$$

$$[K_7] = \begin{bmatrix} -1 & 0 & 1 \end{bmatrix} \cdot \frac{1}{3\omega RC}$$

$[K_6] = [0]$; $[K_8] = [0]$; $[K_{11}] = [0]$;

$[K_{12}] = [0]$; $[K_{13}] = [0]$; $[K_{14}] = [0]$

$[K_{20}] = [0]$; $[K_{22}] = [0]$; $[K_{16}] = [0]$

$$[K_{19}]=\begin{bmatrix}1 & 0 & 2\\ -2 & 0 & -1\end{bmatrix}.(R/3)$$

$$[K_{21}]=\begin{bmatrix}1 & 0 & 2\\ -2 & 0 & -1\end{bmatrix}.\frac{1}{3\omega C}$$

$$[K_{15}]=[K_{19}][K_1]+[K_{20}][K_2]+[K_{21}]$$

$$=\begin{bmatrix}\left(\frac{-R_s}{\omega L_s}+\frac{1}{\omega RC}\right) & 0 & \left(\frac{-2R_s}{\omega L_s}+\frac{2}{\omega RC}\right)\\ \left(\frac{2R_s}{\omega L_s}-\frac{2}{\omega RC}\right) & 0 & \left(\frac{R_s}{\omega L_s}-\frac{1}{\omega RC}\right)\end{bmatrix}.(R/3)$$

$$[K_{17}]=\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}.(R/(3\omega L_s))$$

$$[K_{18}]=\begin{bmatrix}0 & 0 & 1\\ -1 & 0 & 0\end{bmatrix}.(R/(3\omega L_s))$$

The final equation can be obtained by putting these calculated values of submatrices. For other GTO conduction patterns the value of submatrices can be calculated in the same way.

DISCUSSION

The equation (3.26) is formed at each time step. The

changes in the status of GTOs in the link can be considered by rearranging the columns of matrix $[B_L]$. The matrix $[B_L]$ has to be changed as the status of values in branch changes. The method given here is simpler, both conceptually and computationally. Also the GTO characteristics can be assumed different than that of an ideal switch. The constituent equation in this case would be different than equation (3.15). To give an illustration, the impedence of the GTO during nonconduction can be assumed to be finite (determined by the grading and damping circuit). Inclusion of this characteristic can be easily accomplished. In contrast, the reference[15] implicitly assumes the GTO valve impedence to be infinite during nonconducting period. The snubber circuit may also be included but then complexity of graph will be increased. Inclusion of snubber circuit will increase nodes and elements of the graph. In contrast,the reference [3] has implicitly neglected the snubber circuit. The number of state equations per converter vary depending upon the number of conducting GTOs (N) and is given by (N+2).

3.4 COMPUTER PROGRAM

Based on the procedure outlined in the previous sections, a computer program has been developed to validate the converter model. The structure of the program is modular with subsystem described in the individual subroutine. At a particular instant of time, the states of converter are defined and the equations are formulated using the converter model described

earlier. The converter state changes due to the extinction of the GTOs or the firing of the GTOs. The converter state is checked at the begining of each integration time step. The presence of firing pulse indicates the conducting GTO which is generated by pulse generating subroutine and the GTO is put into the conducting state if it is high and the GTO is put into nonconducting state if it is zero. The salient feature of the program is given below. The flow chart of the program is given in Figure (3.6).

INITIAL CONDITIONS

The simulation can proceed from a) zero initial conditions or b) initial conditions established from the steady state operating point. For the second case the required steady state operating conditions are calculated. The present program uses the EPWM firing scheme. The program can be run more than a cycle. The voltage of ac supply, frequency of supply, transformer leakage impedance , smoothing impedance, step of integration, output voltage pulse per ac cycle, modulation index and reduced bus incidence matrix have to be given as the input datas. The analysis is started assuming that the GTOs G_6 and G_3 are in conduction prior to turning on of G_1 at α_1 which is calculated by expression given in table (2.1) for EPWM. The conduction pattern of the GTOs are given in the Appendix V for symmetrical gating of EPWM scheme. The initial conditions required for the numerical integration can be fed externally or determined by the program using following relations.

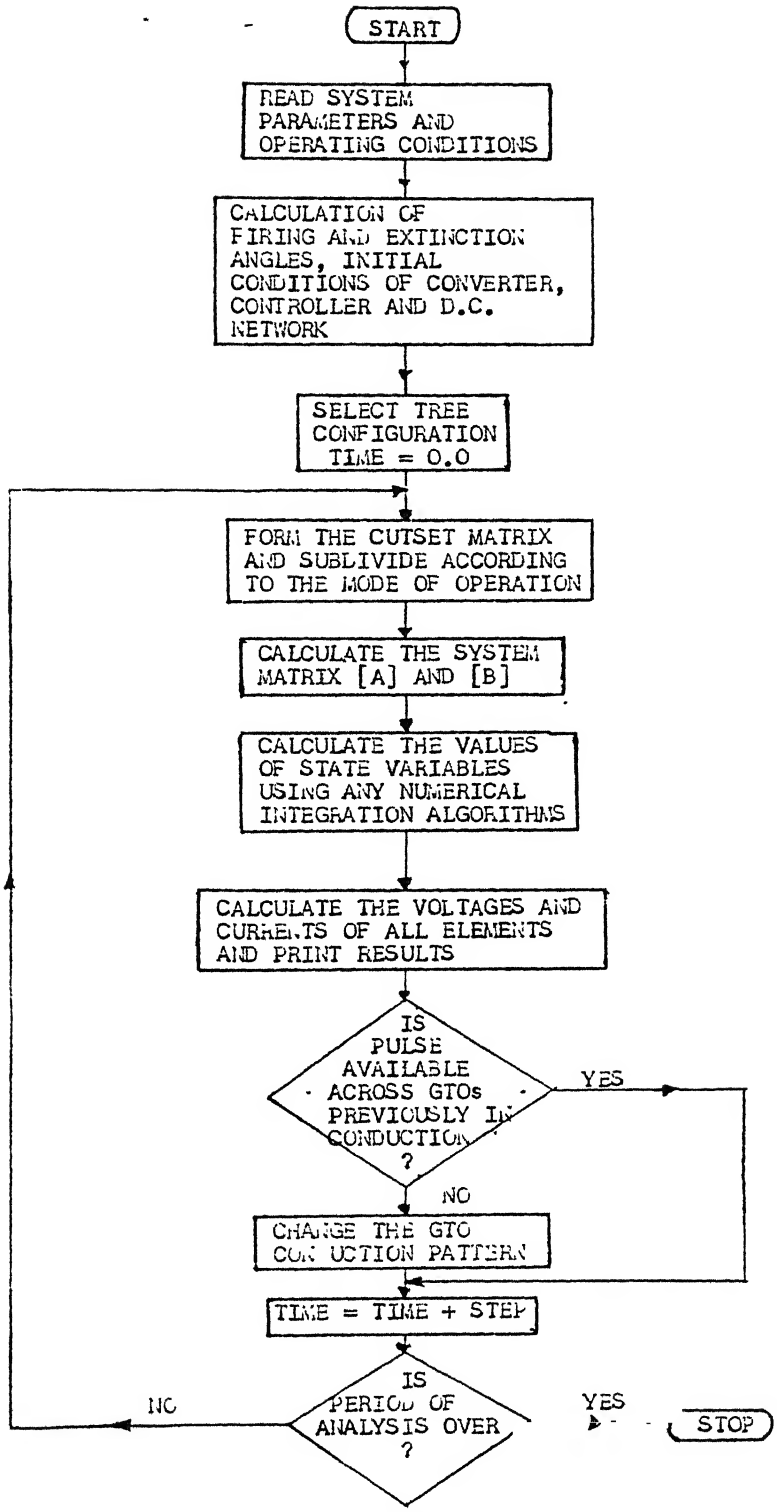


Fig. 3.6 FLOW CHART

Initial load current as

$$I_d(0)=i_8(0)= 0.8*(E_d-E_b)/R_d$$

where E_0 is the average output voltage and can be calculated by using equation (I.4). Other initial conditions can be calculated as follows,

$$i_7(0)= 0.0$$

$$i_9(0)= 0.0$$

$$V_{10}(0)= e_1-e_2$$

$$V_{11}(0)= e_2-e_3$$

3.5 TEST SIMULATIONS

The capability of the program developed is illustrated by simulating the GTO converter with an active load. The details of the system parameters are given in Appendix IV. The test simulations are carried out to investigate the system response in steady state for both modes of converter (rectification/inversion).

Figure (3.7) shows the steady state output current of rectifier and the ac phase 'A' current is shown in Figure (3.8). The valve voltages across G_1 and G_2 are given in Figure (3.9) to Figure (3.10). Figures (3.11) to (3.13) show the current through GTO valve 1, current through transient suppressor circuit and dc output voltage of rectifier operation. The voltage across transient suppressor circuit elements are given in Figures (3.14) & (3.15).

Figures (3.16) to (3.21) show the result obtained from inverter operation of GTO converter. The input dc voltage applied

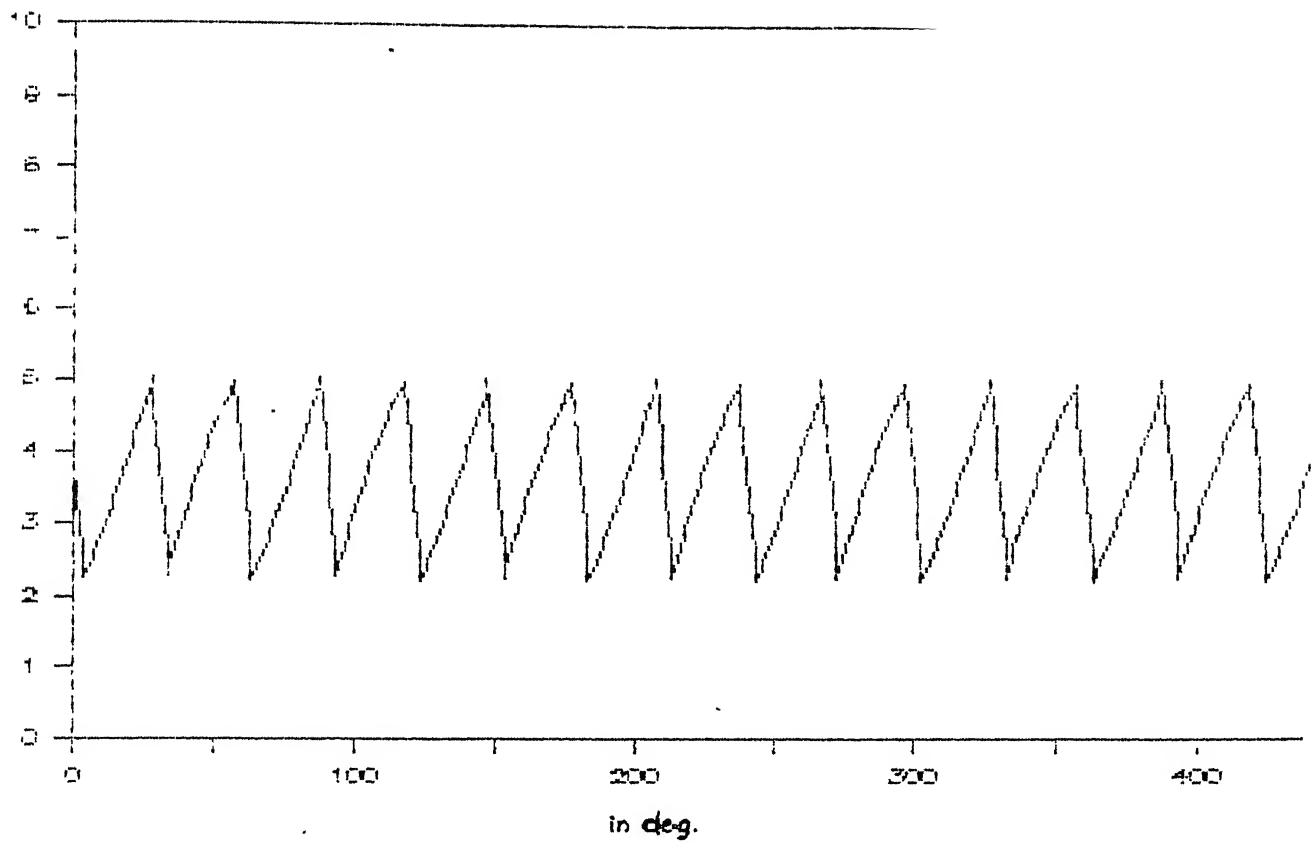


FIG. 3.7 RECTIFIER DC CURRENT

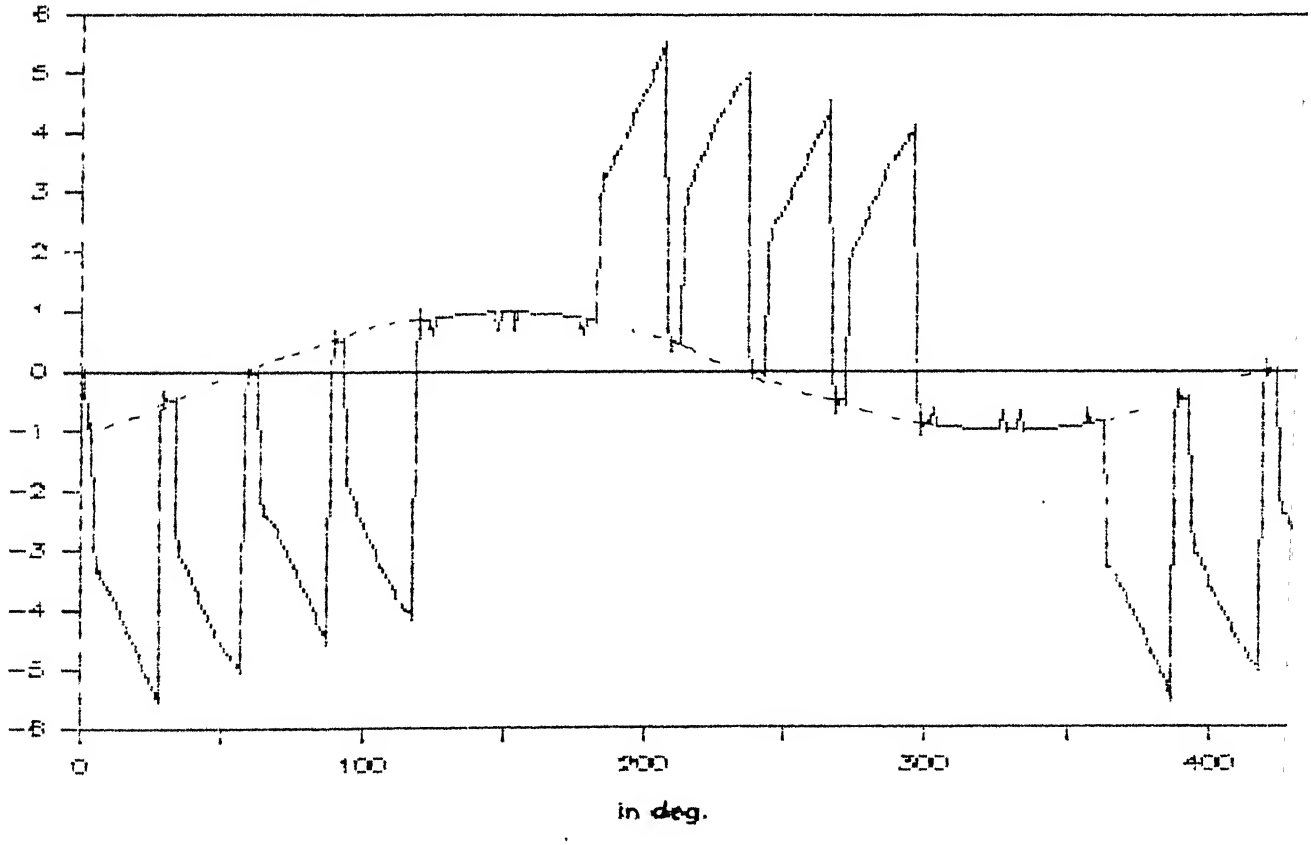


FIG. 3.8 RECTIFIER PHASE 'A' CURRENT

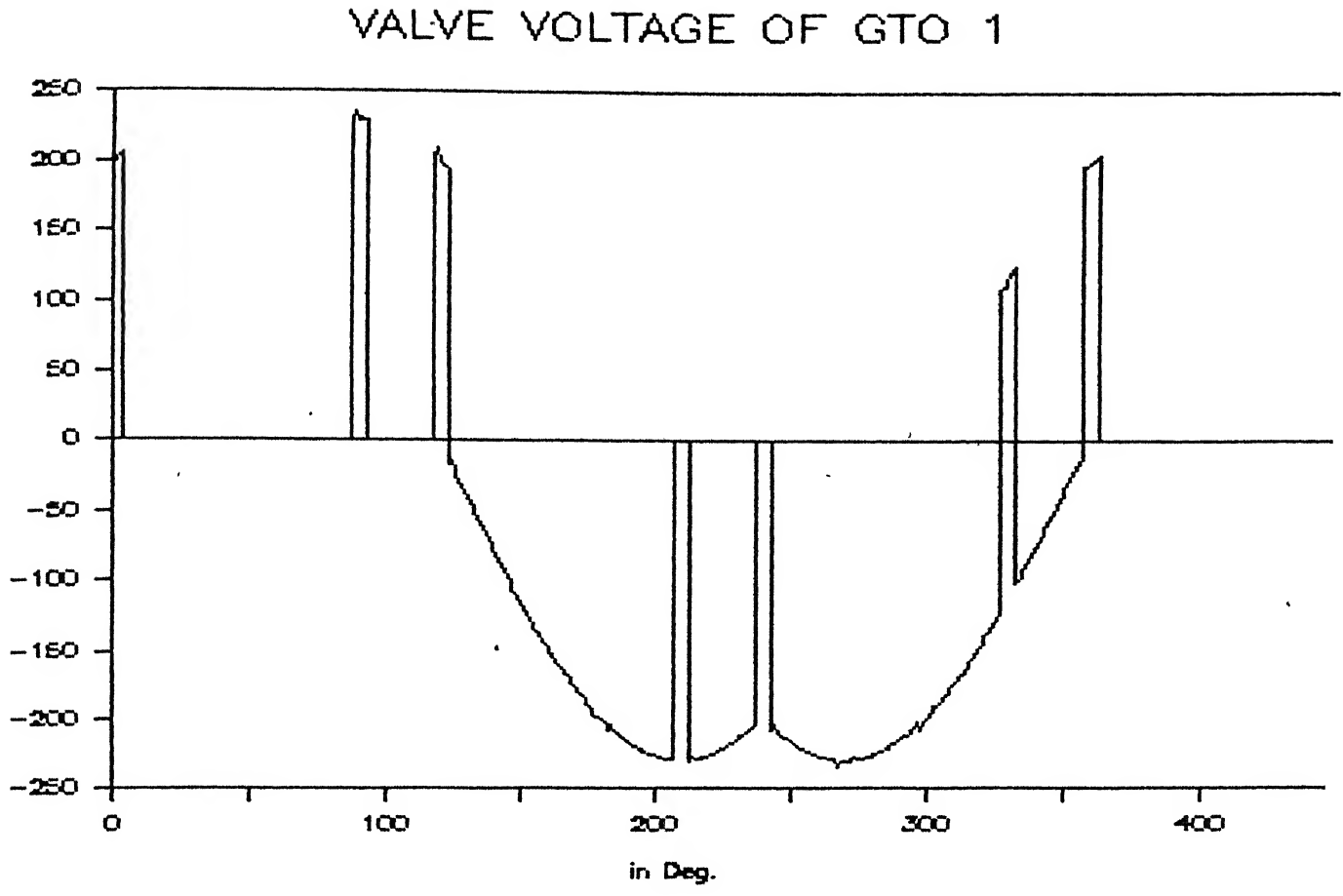
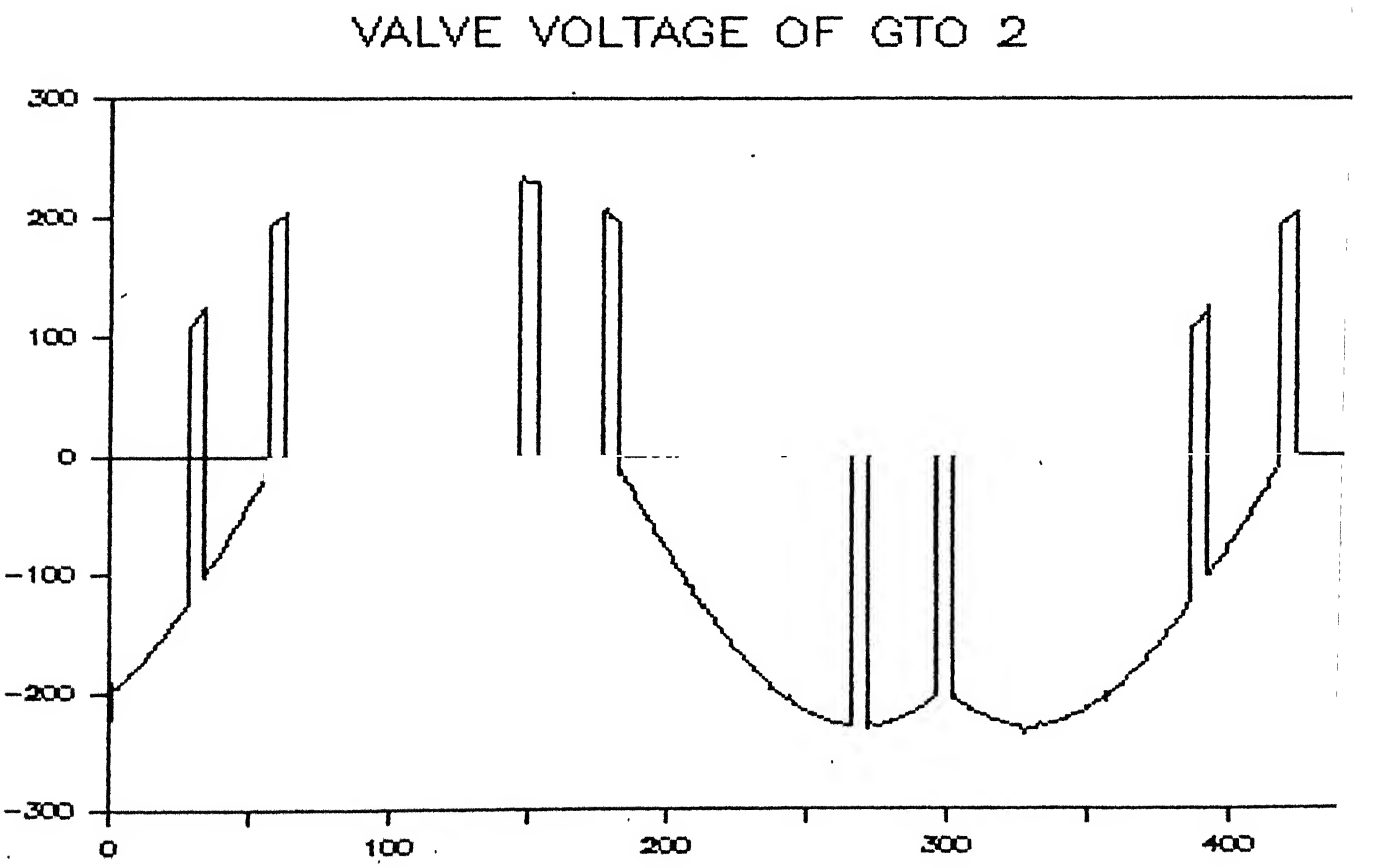


FIG. 3.9 VOLTAGE ACROSS GTO VALVE-1



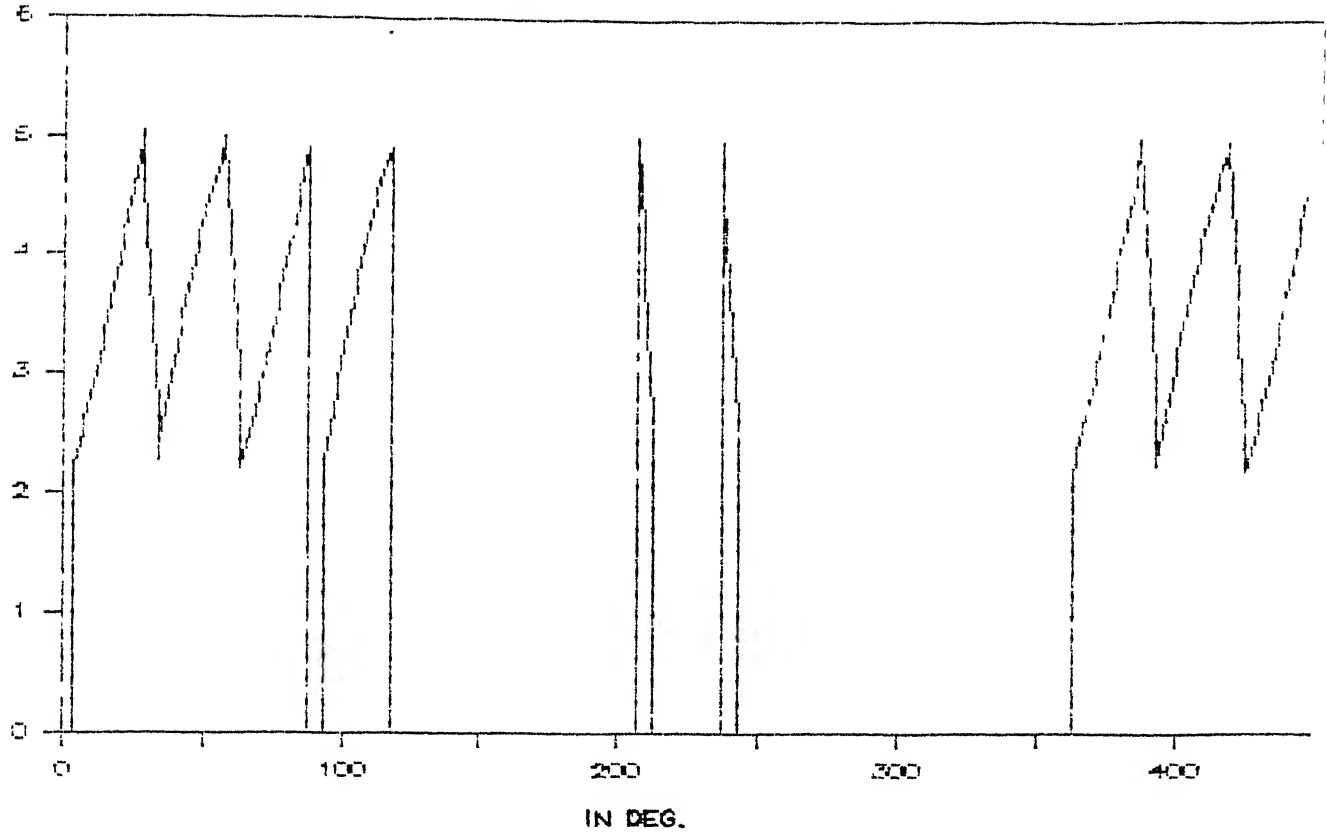


FIG. 3.11 CURRENT THROUGH GTO VALVE-1

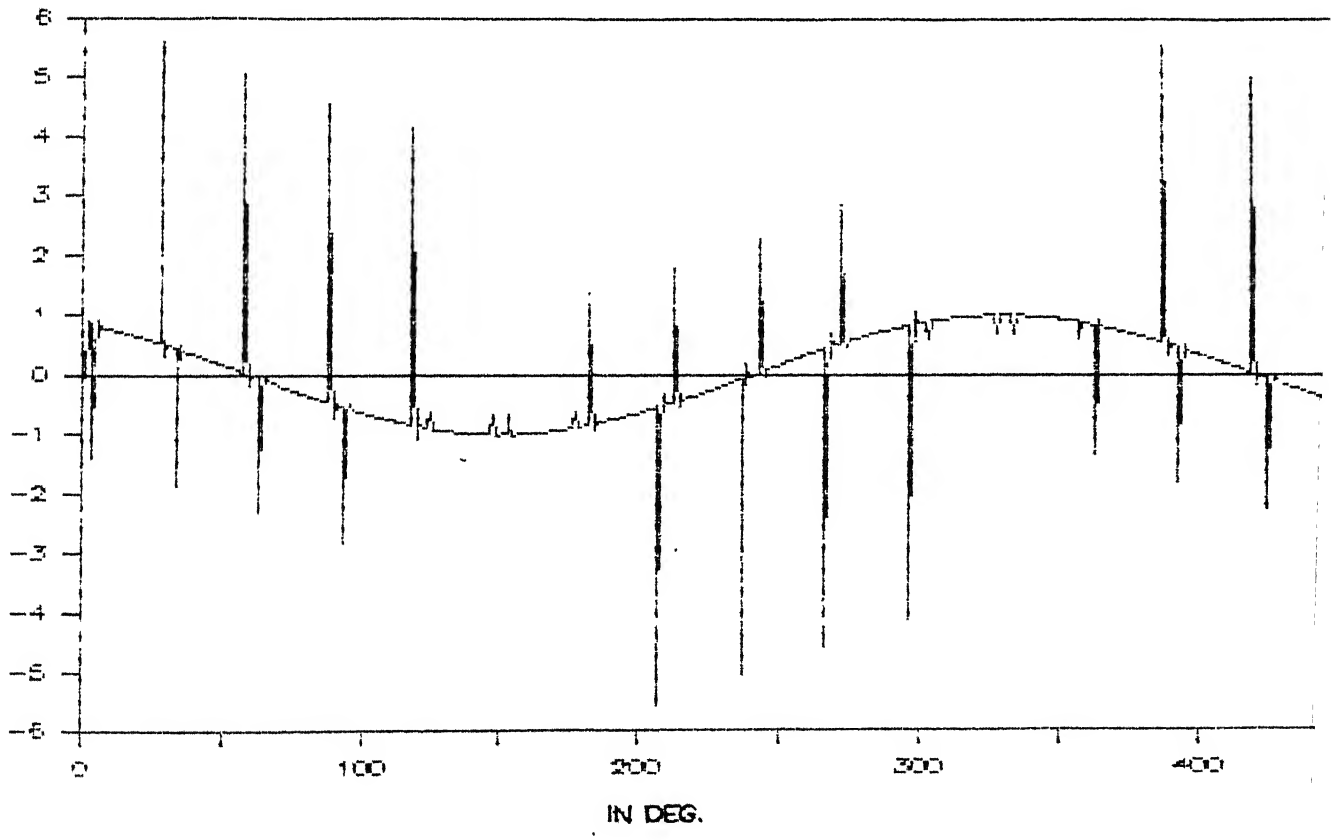


FIG. 3.12 CURRENT THROUGH TRANSIENT SUPPRESSOR CIRCUIT

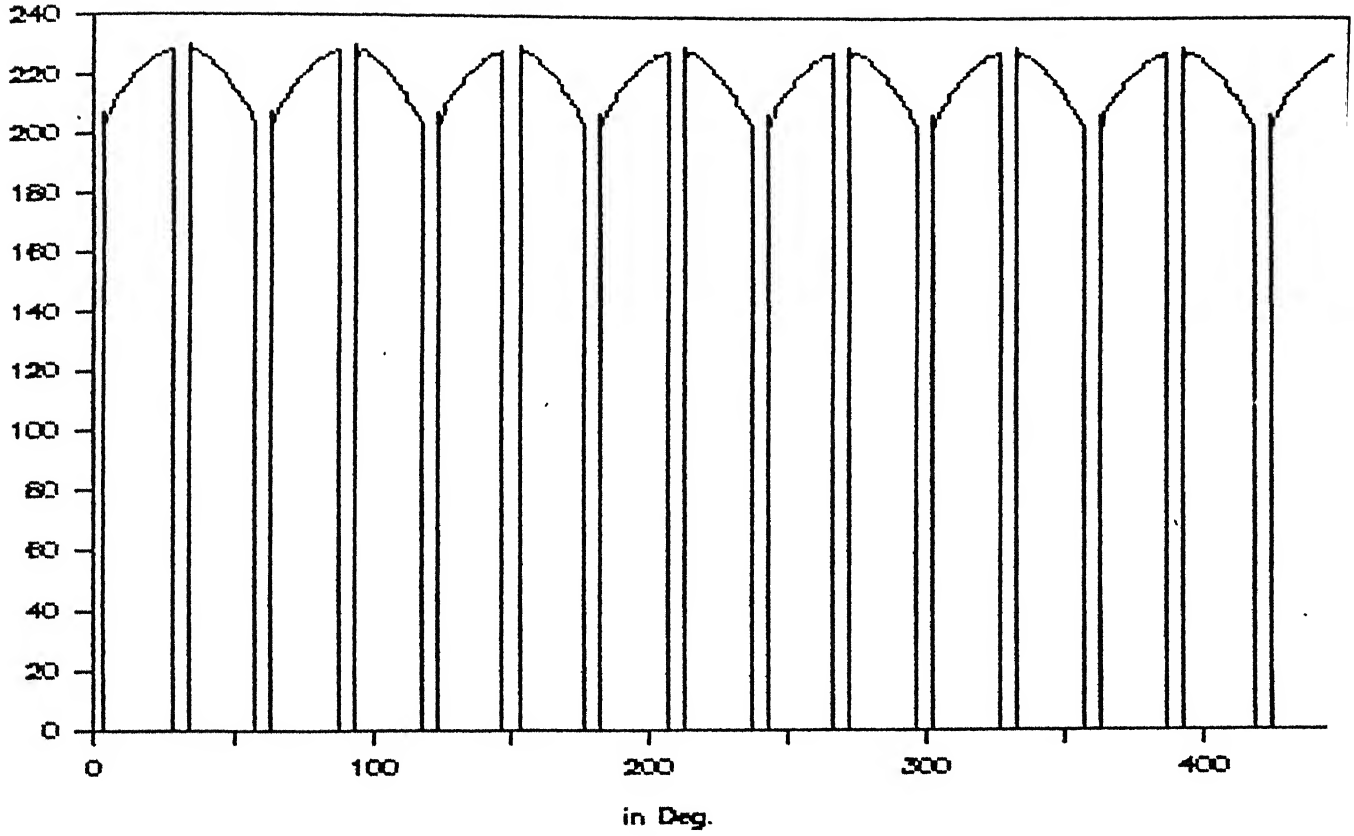


FIG. 3.13 RECTIFIER DC VOLTAGE

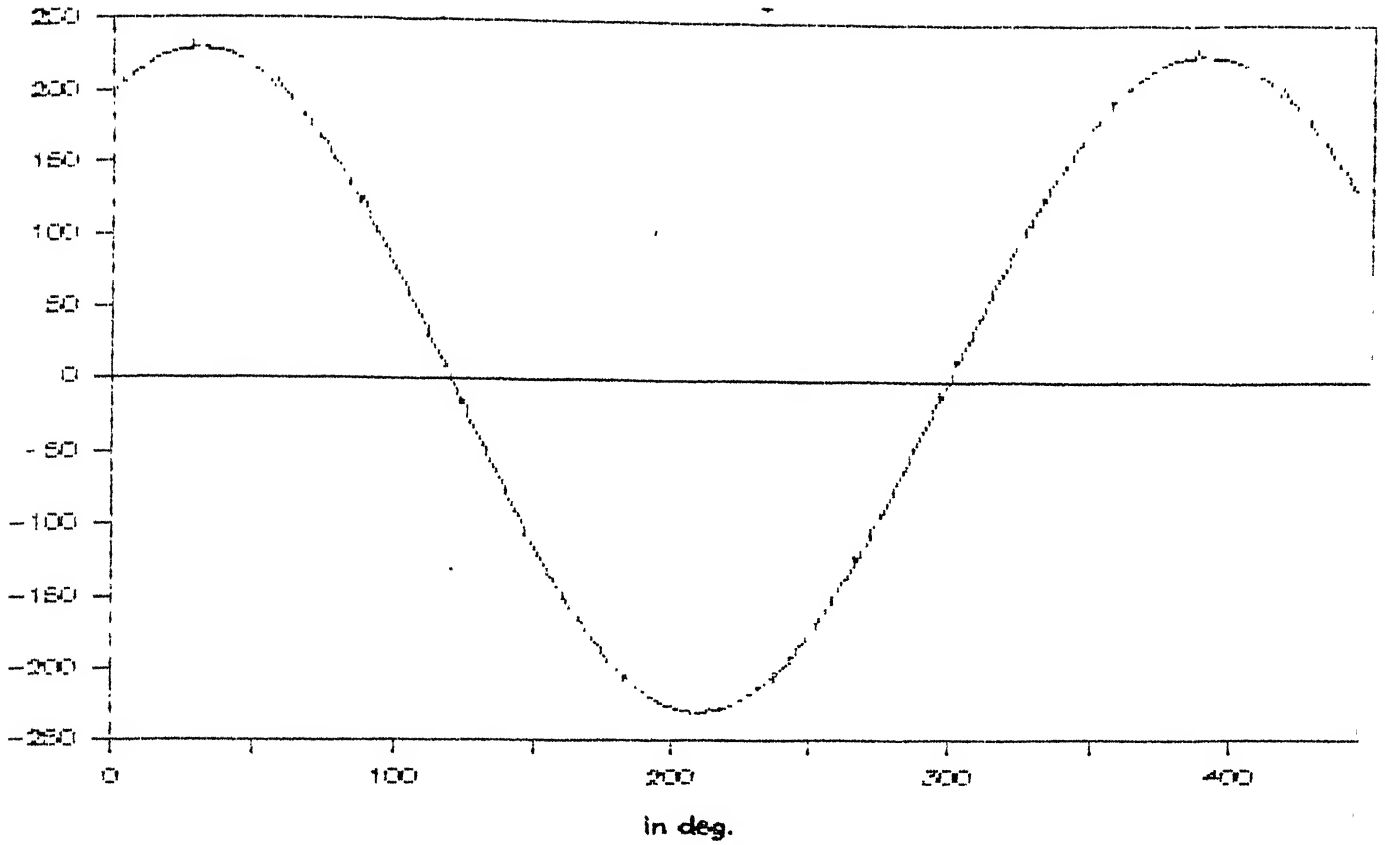


FIG. 3.14 VOLTAGE ACROSS TRANSIENT SUPPRESSOR CIRCUIT

(PHASE A-B)

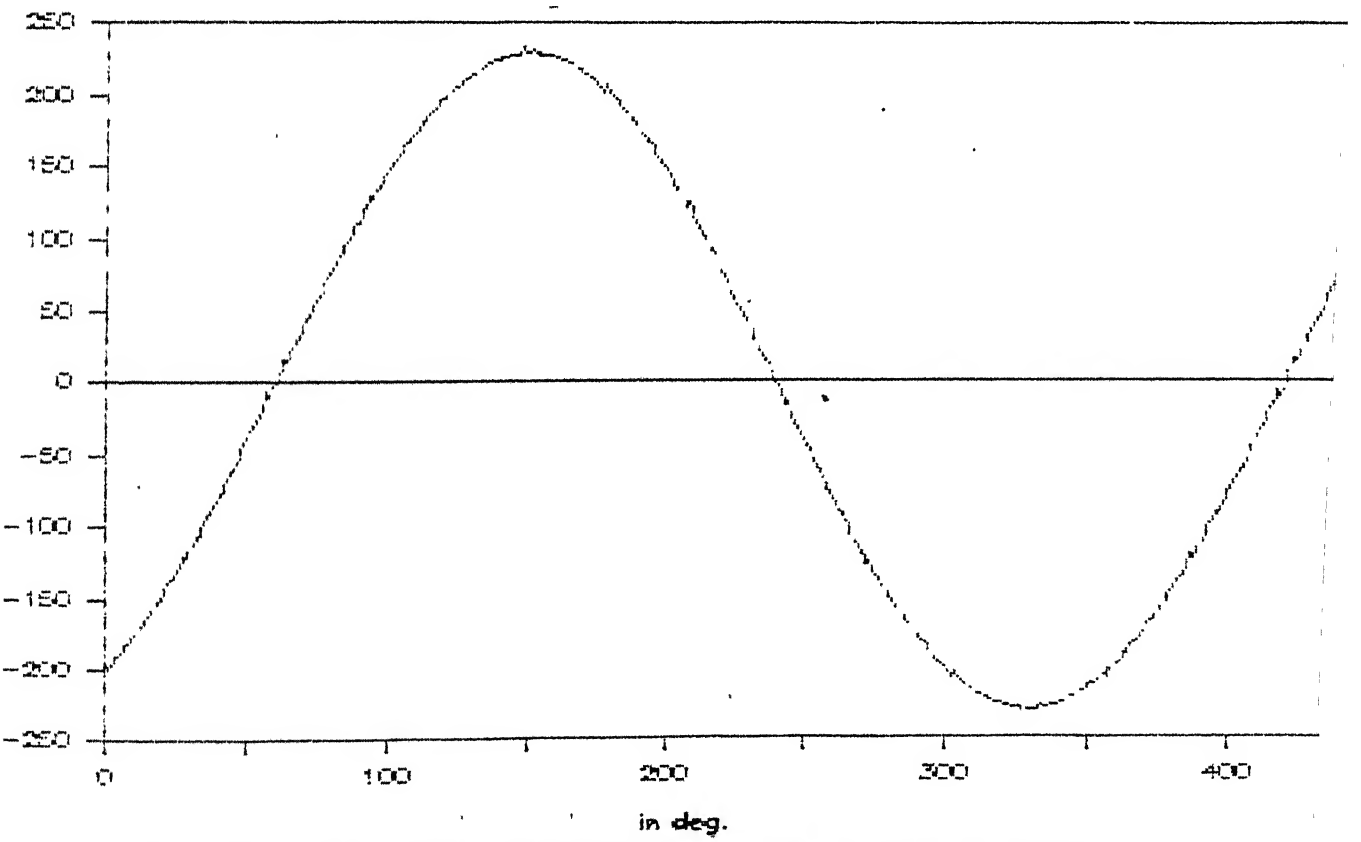


FIG. 3.15 VOLTAGE ACROSS TRANSIENT SUPPRESSOR CIRCUIT

to the inverter is 180.0 volts with negative polarity and other parameters remain same. Figure (3.16) shows the ac output current from inverter. The waveform of dc current flowing through this is shown in Figure (3.17).The current through GTO valve 1 and suppressor circuit is shown in Figures (3.18) and (3.19) respectively. The voltage across GTO valve 6 and across transient suppressor circuit are also given in Figures (3.20) and (3.21) respectively.

The harmonic analysis of rectifier operation of GTO converter is also presented under assumption mentioned in previous sections. This is done by discrete fourier analysis. The X-Axis of graph represents the multiple of fundamental frequency. The Y-Axis shows the magnitude of harmonics. Figure (3.22) shows the harmonic components of ac voltage and Figure (3.23) shows the harmonics in ac phase current. The harmonics components of dc sides voltage and current are shown in Figures (3.24) and (3.25) respectively.

DISCUSSION OF RESULTS

The results demonstrate the operation of converter (rectifier / inverter) under steady state. In Figures (3.7) and (3.16), a ac current of 1 ampere (approx.) flows continuously which leads the phase current by an angle of 90^0. This is only due to the RC transient suppressor circuit, present at converter ac bus. The value of C must be chosen judiciously so that it should not load the ac source substantially. The value of R and C can be

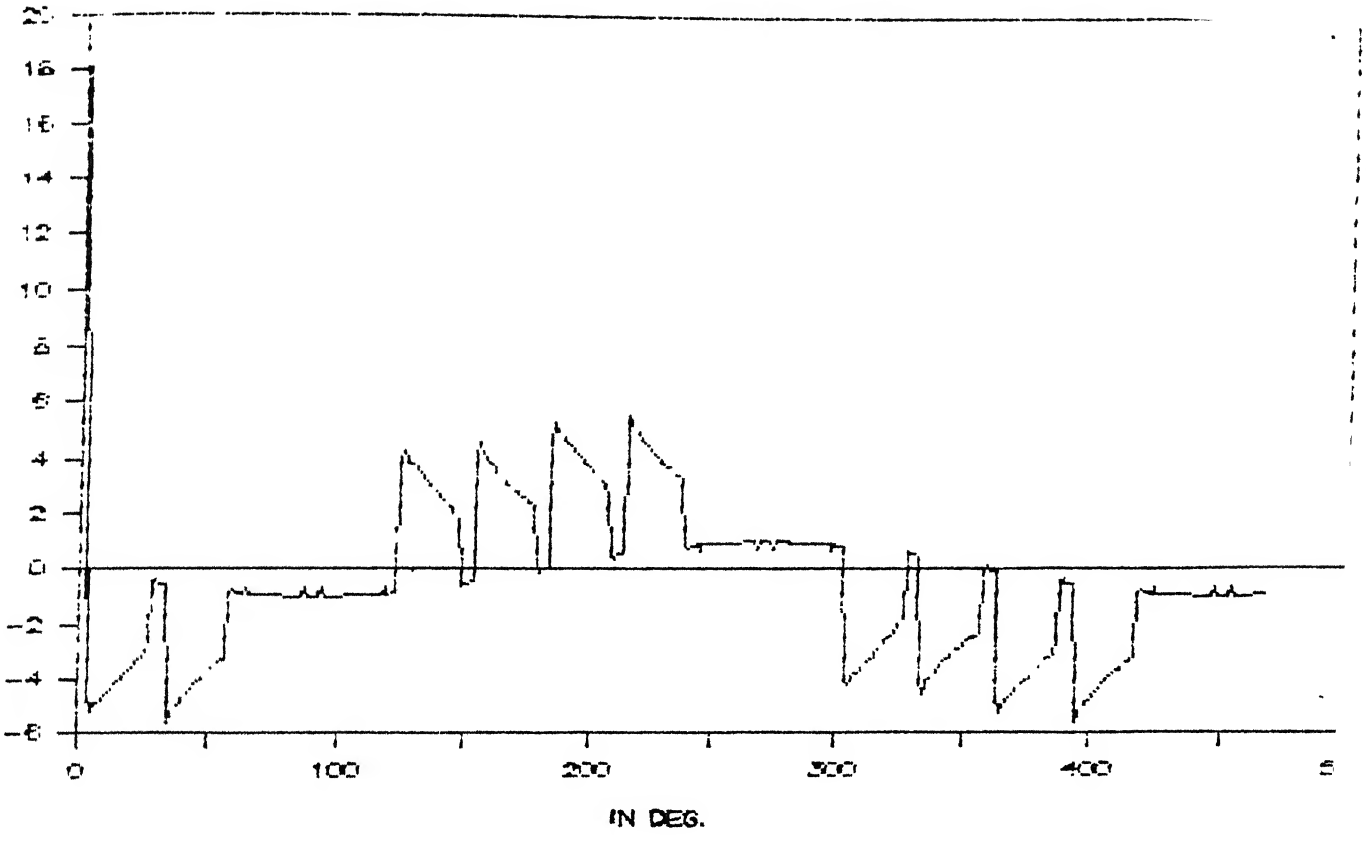


FIG. 3.16 INVERTER PHASE 'B' CURRENT

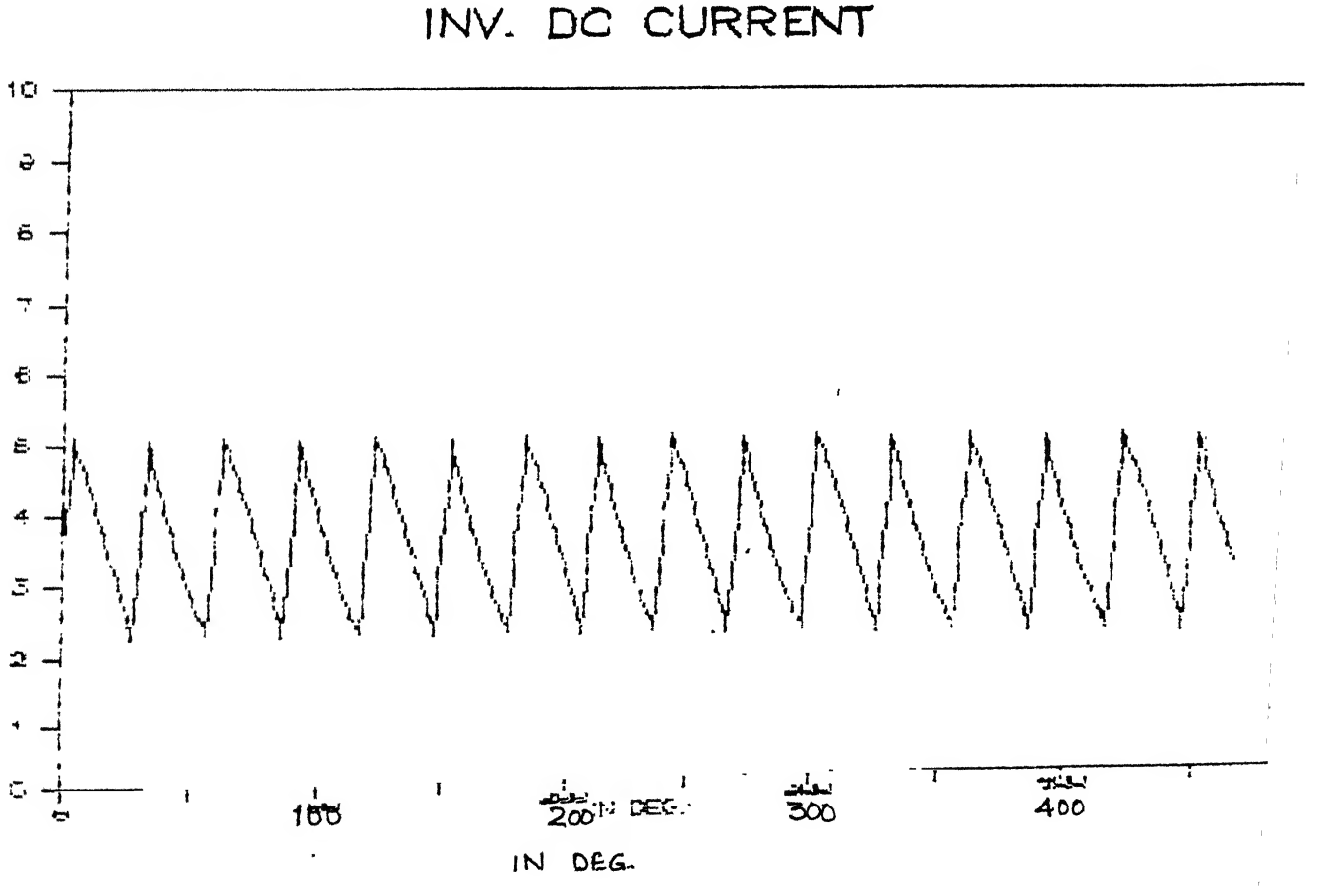


FIG. 3.17 INVERTER DC CURRENT

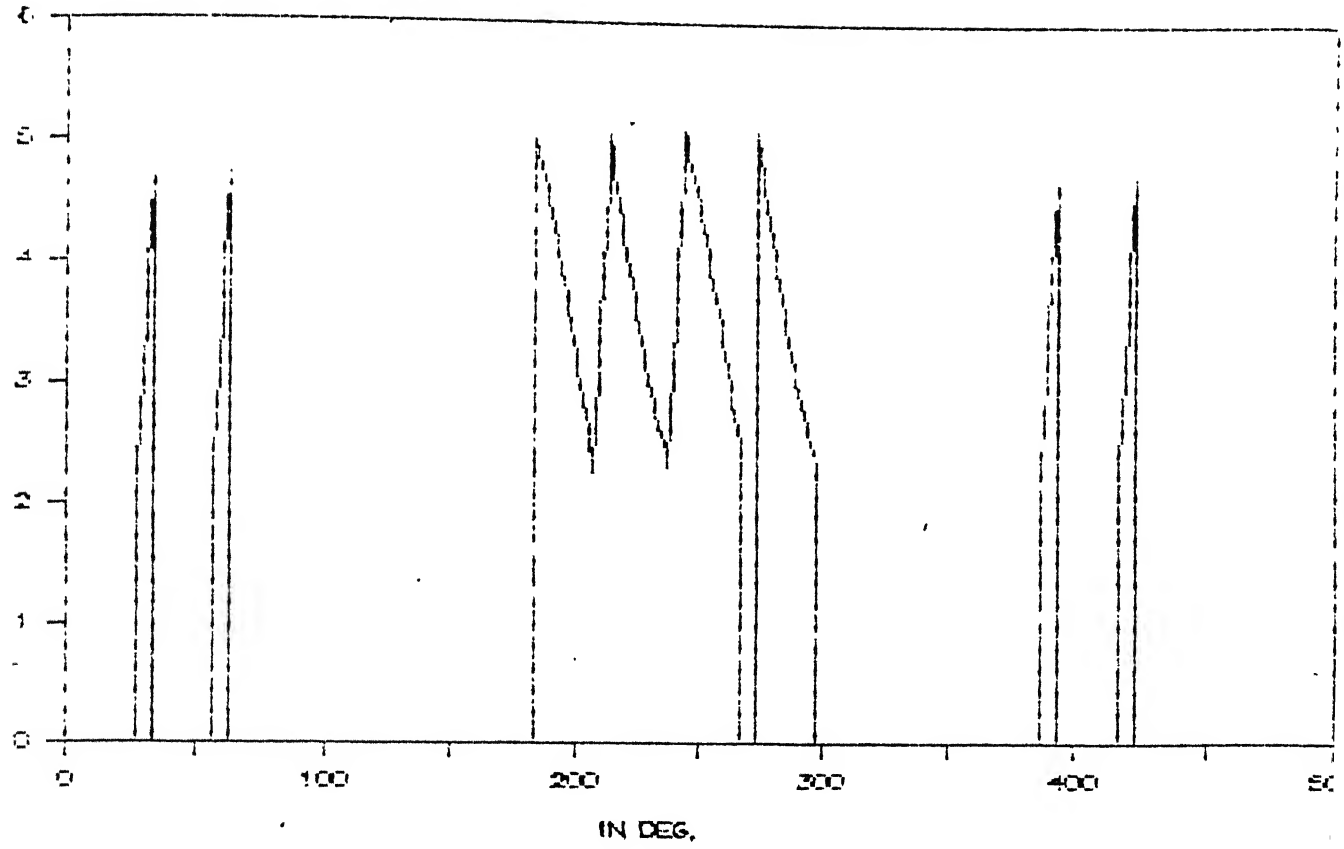


FIG. 3.18 CURRENT THROUGH GTO VALVE-1

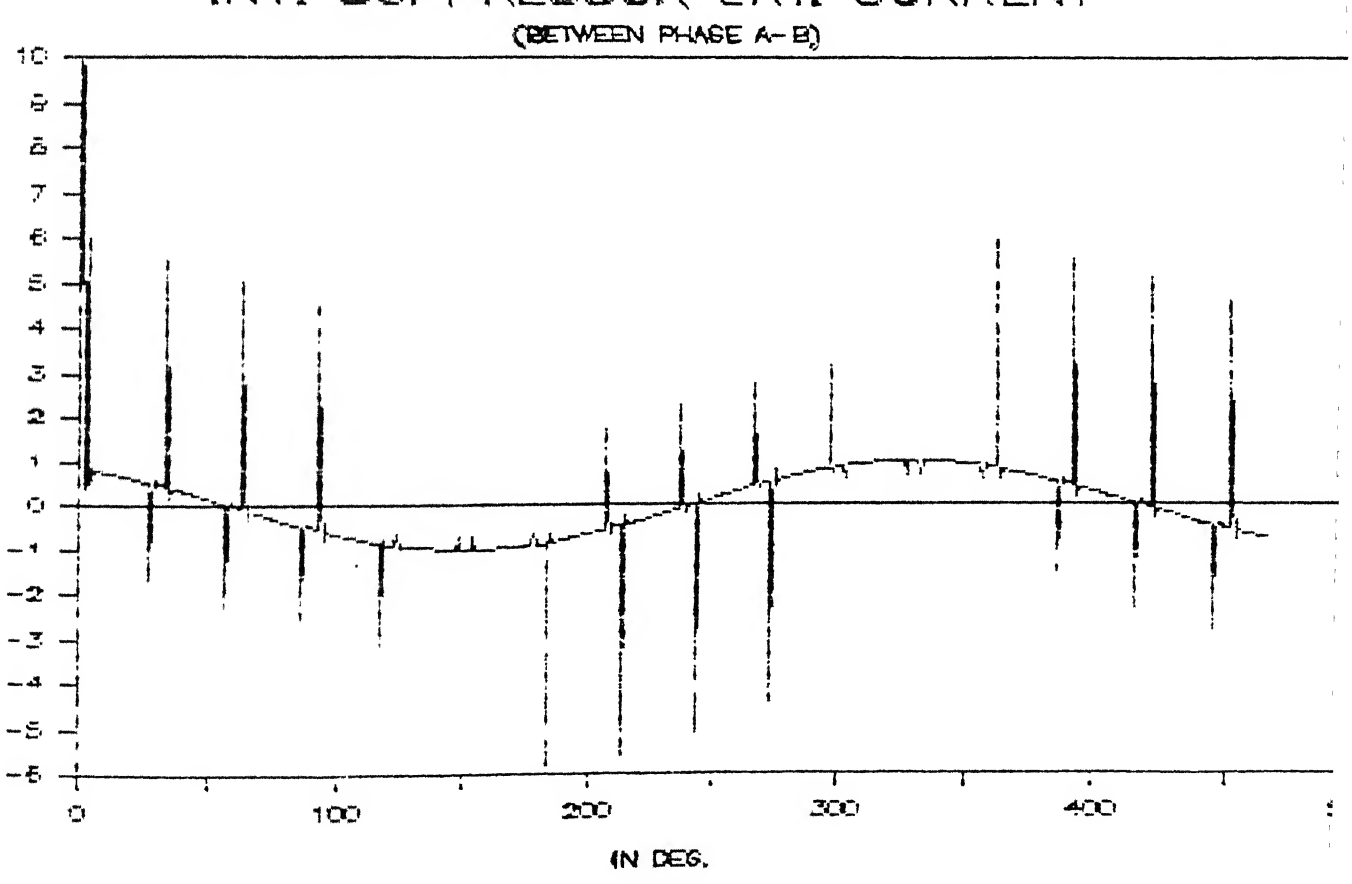


FIG 3.19 CURRENT THROUGH TRANSIENT SUPPRESSOR CIRCUIT

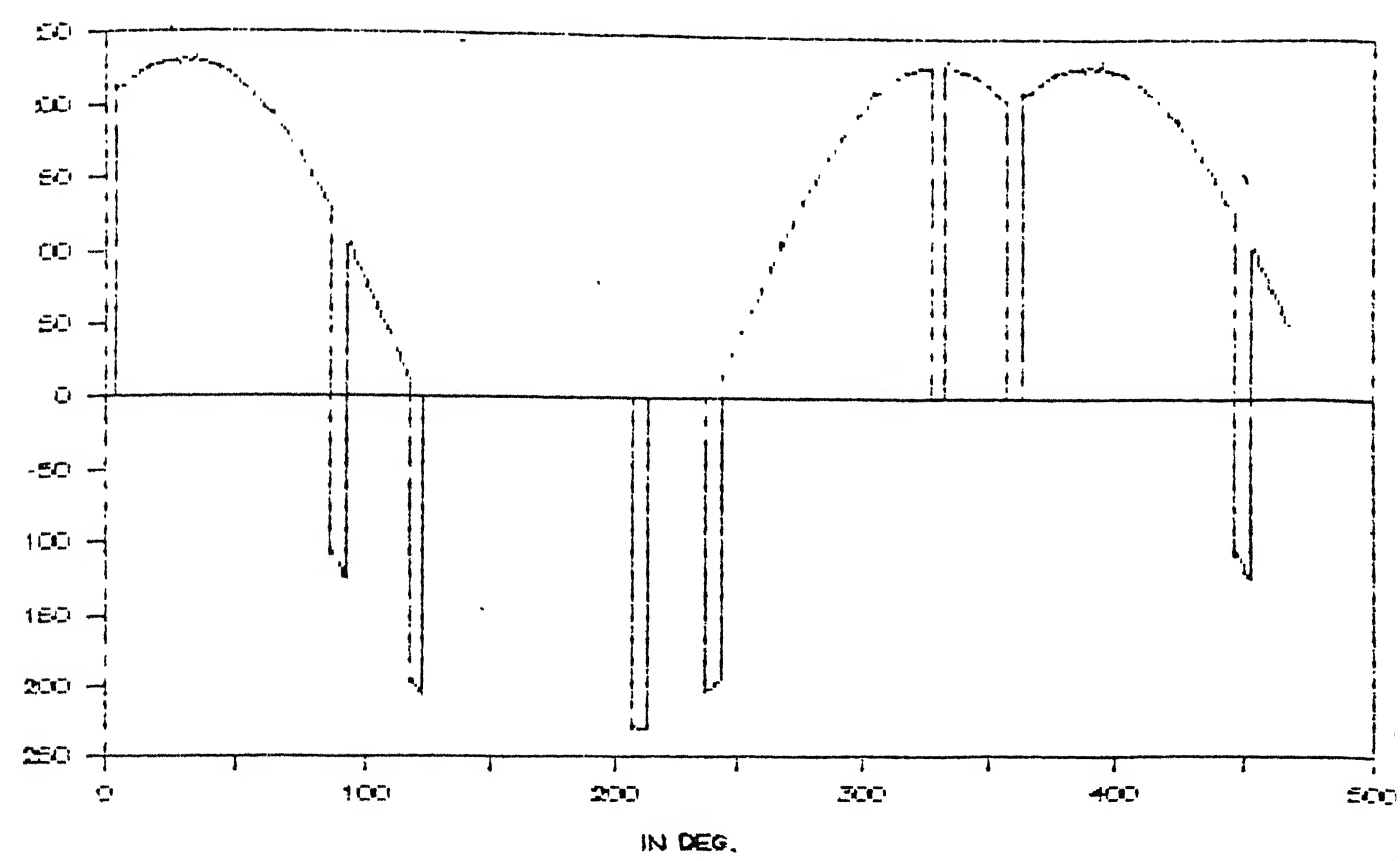


FIG. 3.20 VOLTAGE ACROSS GTO VALVE-6

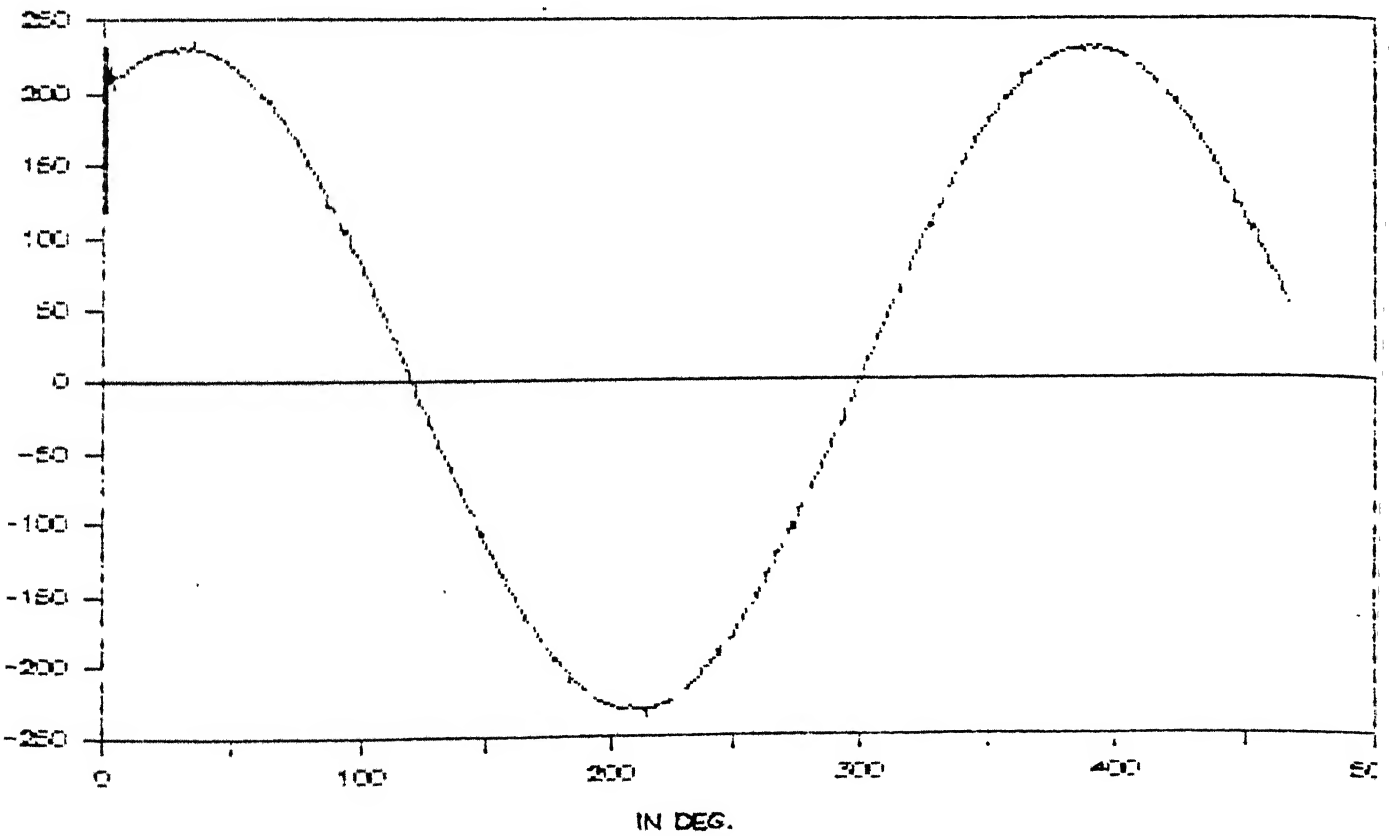


FIG 3.21 VOLTAGE ACROSS TRANSIENT SUPPERSSOR CIRCUIT

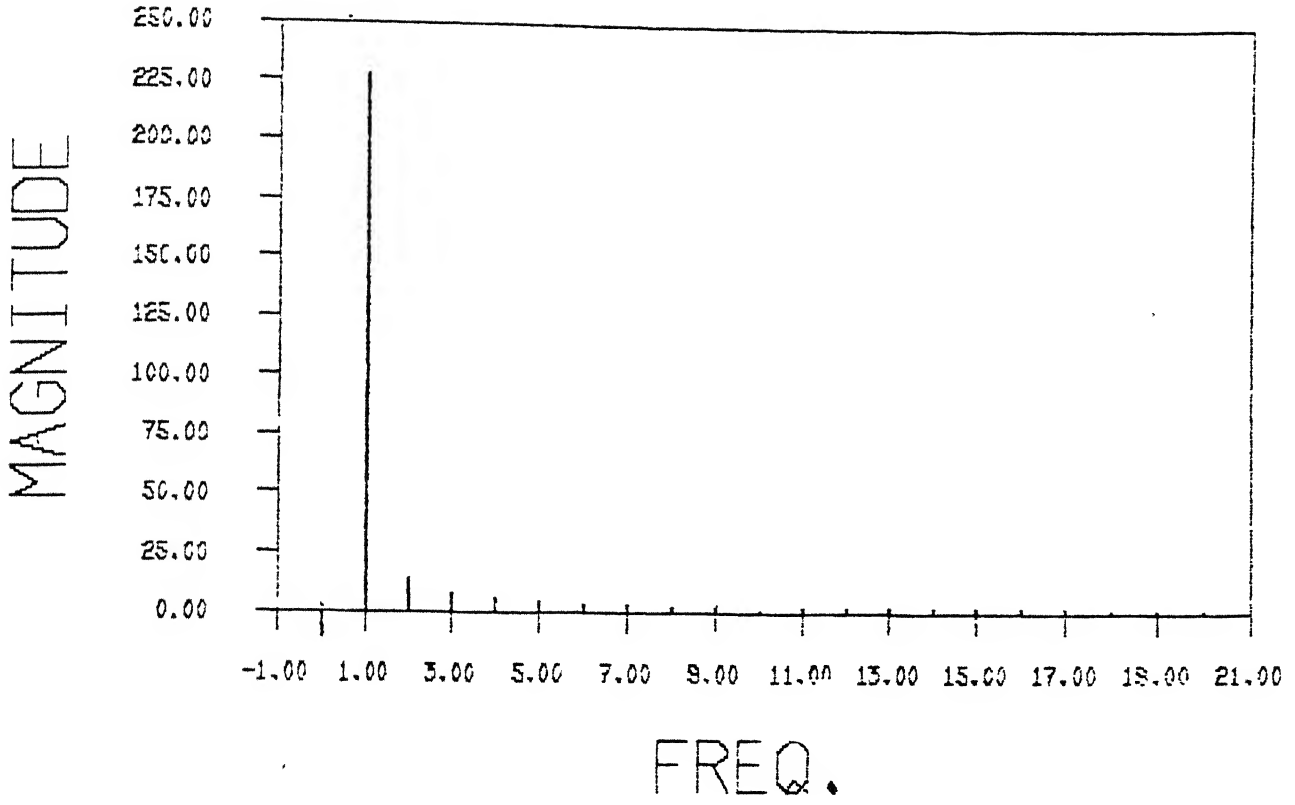


FIG. 3.22 HARMONIC COMPONENTS OF RECTIFIER AC VOLTAGE

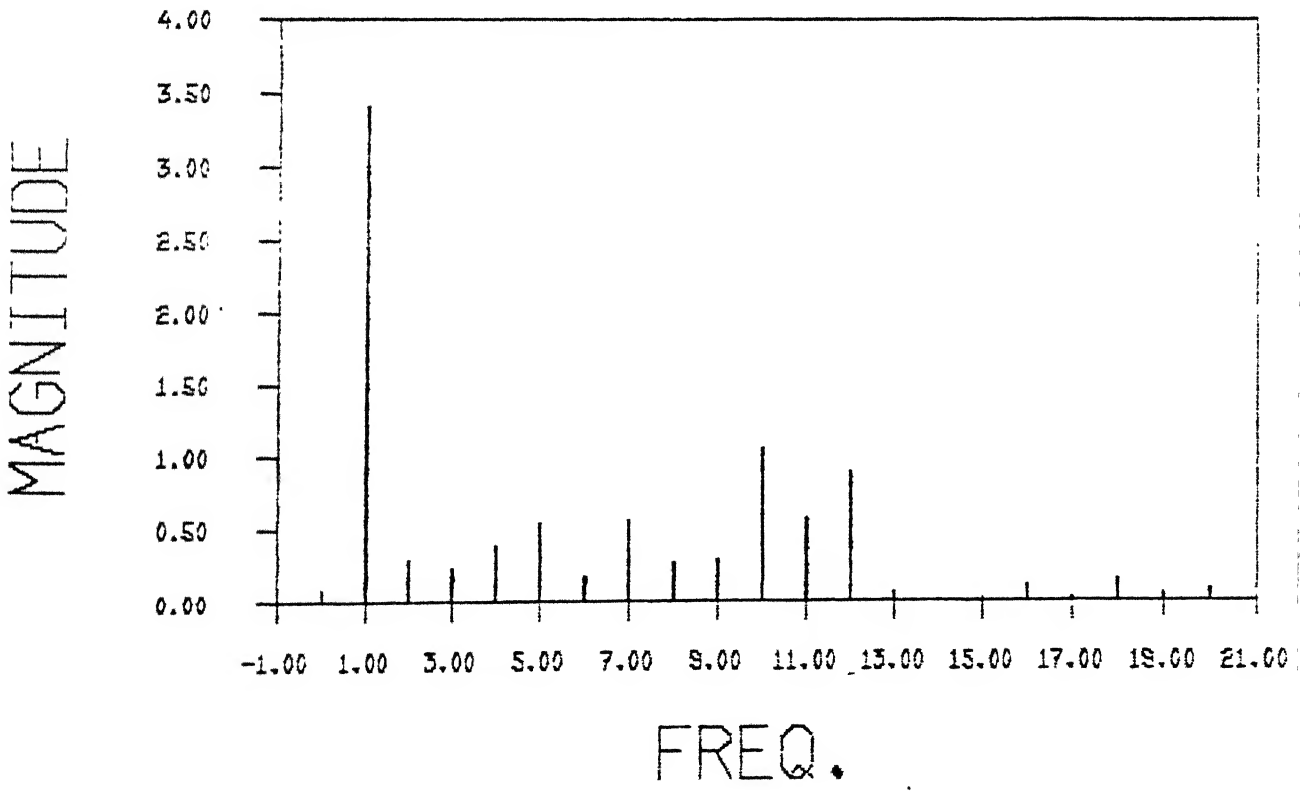


FIG. 3.23 HARMONIC COMPONENTS OF RECTIFIER AC CURRENT

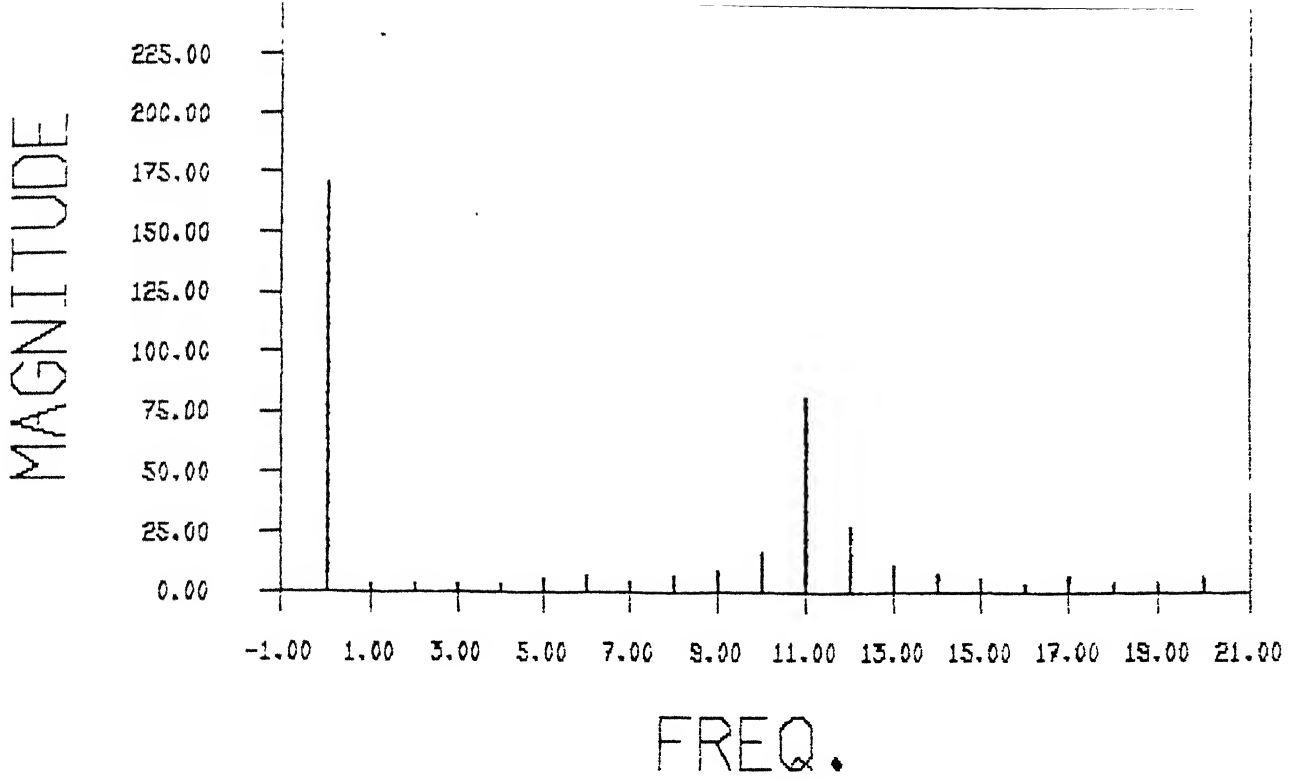


FIG. 3.24 HARMONIC COMPONENTS OF RECTIFIER DC VOLTAGE

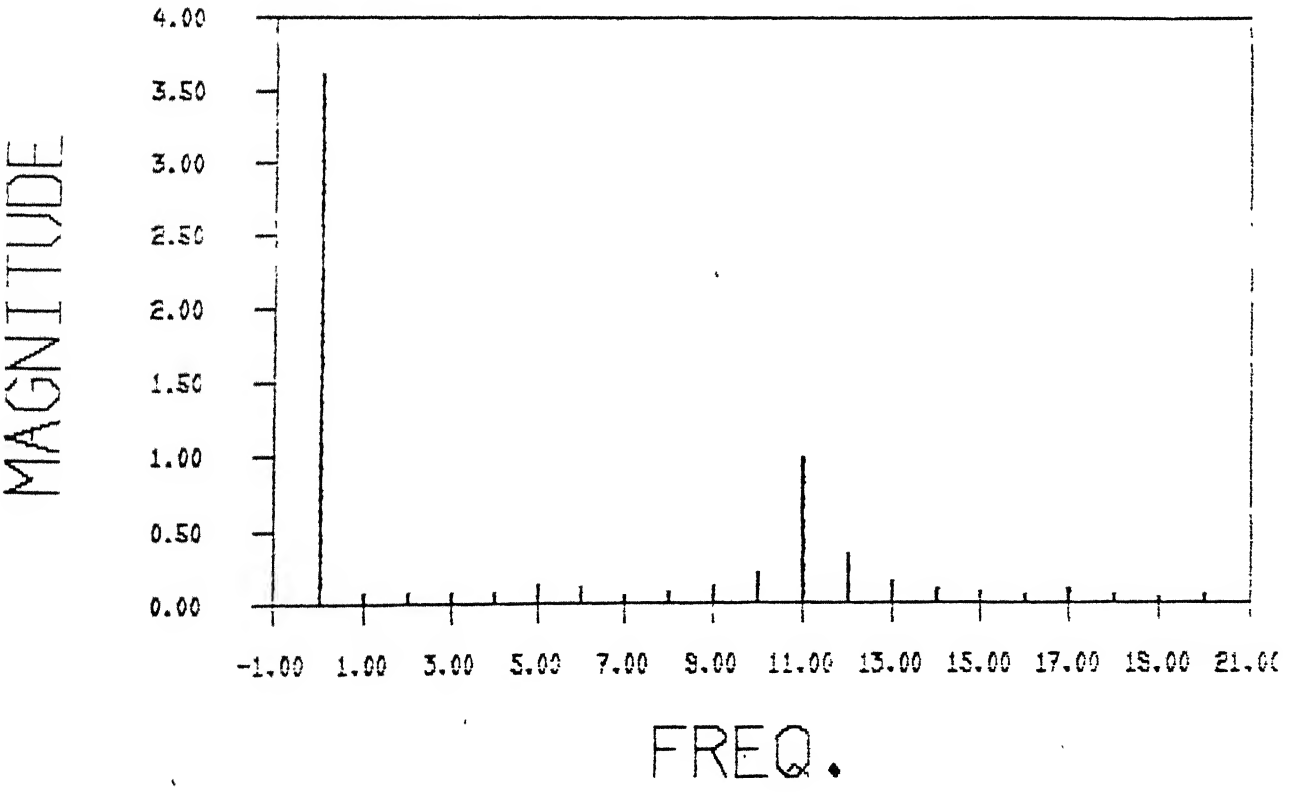


FIG. 3.25 HARMONIC COMPONENTS OF RECTIFIER DC CURRENT

optimized accordingly but this optimisation is not attempted here. The spikes present are due to change over of GTO conduction pattern which causes the interruption of source current. The dc current has ripples. The current rises in power mode and falls in free wheeling mode. This rise and fall will depend on the value of resistances and inductances present in the dc current path. Apart from fundamental component in ac voltage are not of significant magnitude. The hormonics present in source current are 2nd to 12th however, the magnitudes of 5th ,7th, 10th and 12th are higher than others. The magnitudes of harmonics are dependent of:

1. method of modulation and number of pulses per cycle of source voltage.
2. nature of loads
3. presence of source impedance and
4. presence of RC transient suppressor circuit.

The harmonic in dc side is only 11th, although 10th, 12th and 13th are also present but their magnitudes are lower than 11th.

3.6 CONCLUSION

In this chapter a state space model for the three phase ac-dc PWM GTO converter system has been developed based on the graph theoretic approach. The generalise set of state equations has been derived based on the network cutest matrix. The system model is general enough to be used for investigation of performance for three or more GTO conduction at a time. A simulation program has been written to validate the model

developed. The test simulation has been carried out with given parameters for 12 pulse per cycle of source voltage.

CHAPTER 4

GTO INVERTER IN HVDC LINK

4.1 INTRODUCTION

An HVDC system, with thyristor rectifier and their associated controls, dc network consisting of transmission line and GTO inverter with controls are discussed in this chapter. Digital simulation requires adequate representation of the various components. This chapter describes the modelling of the constituents of an HVDC system in brief. Emphasis is laid on interfacing of GTO inverter and its controls in place of thyristor inverter using appropriate interfacing variables. A suitable model for GTO has been developed in previous chapter. These models are used for digital simulation to study the performance of HVDC link with GTO inverter. The simulation has been carried out with ac system representation. A computer program is used to carry out a large number of test simulations, both under steady state and transient conditions, to demonstrate the feasibility of GTO inverter in two terminal HVDC link. The disturbances considered,to study the dynamic behaviour, are change in current reference setting and ac voltage dips at both rectifier and inverter terminals.

4.2 CONVERTER REPRESENTATION

A six pulse thyristor converter is modelled as a

variable voltage source behind a variable impedance. Reference [17] describes the development of an equivalent circuit for a six pulse thyristor converter. This is based on graph theoratic approach which enables to formulate the converter equations for all possible modes of operation assuming continuous dc link current. Converter equations are derived using cutset matrix and the basic circuit equations. The voltage source (e_{eq}) in the equivalent circuit is a function of ac bus voltage and hence has to be computed at each time instant. The equivalent circuit parameters R_{eq} and L_{eq} are dependent on the converter conduction pattern and are recalculated every time when the conduction pattern is changed. The V_c has been included to represent the effect of the dc system. Both ac and dc voltage sources are not constant. R_d and L_d denote the resistance and inductance of smoothing reactor. The thyristor converter equivalent circuit is shown in Figure (4.1). The thyristor converter is used as controlled rectifier.

The GTO converter is used as inverter in HVDC link. The detailed representation of the GTO converter is given in chapter 3.

4.3 DC SYSTEM REPRESENTATION

The dc system comprises of the filters and transmission line. The transmission line is modelled as $\pi-$ equivalent circuit with the shunt arms consisting of capacitors and the series arm a combination of resistance and inductance. A more practical

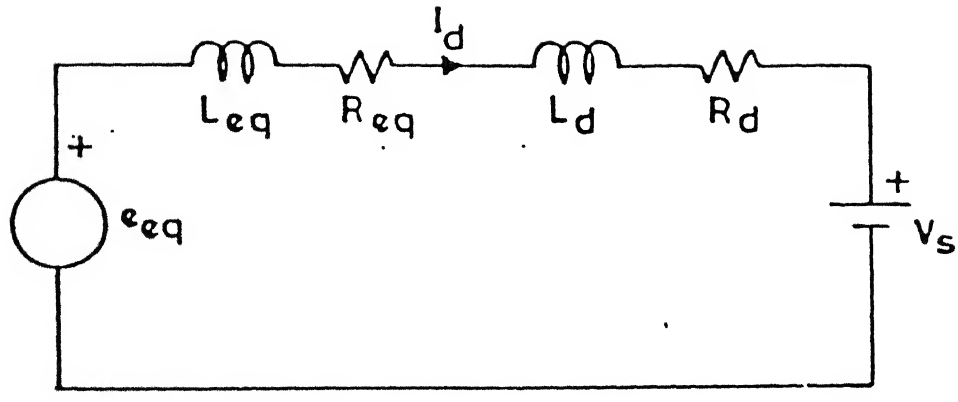


FIG. 4.1 EQUIVALENT CIRCUIT OF 6 PULSE CONVERTER

representation of the line is a number of π-sections. This is achieved by dividing the line into a number of sections, representing each section by its own π-network and connecting all such networks in series. In the dc system representation, the converters are represented as current sources as shown in Figure (4.2). The dc filter used for filtering any harmonics present in the dc current at rectifier end is represented in the dc system model. The dc filter at inverter end is not represented.

4.4 RECTIFIER END CONTROLS

Generally, rectifier is equipped with a constant current controller. The control of the rectifier considered here is based on digital control technique proposed by Freris et al [16]. The firing scheme is basically an Equidistant Pulse Control (EPC) with pulse frequency control (PFC). The interfiring period (IFP), which is the interval between two successive firing instant, is calculated as

$$IFP = 60^{0} + Q_i$$

Where Q_i is the firing correction, calculated by controller. In steady state, Q_i=0 and firing takes place at 60^{0} intervals for a six pulse rectifier. Figure (4.3) shows the block diagram for calculation of Q_i and IFP for constant current control. In the case of constant current control

$$Q_i = K.V_c$$

where K is the gain and V_c is the control signal. The control signal V_c may be a linear function of current error, in which case

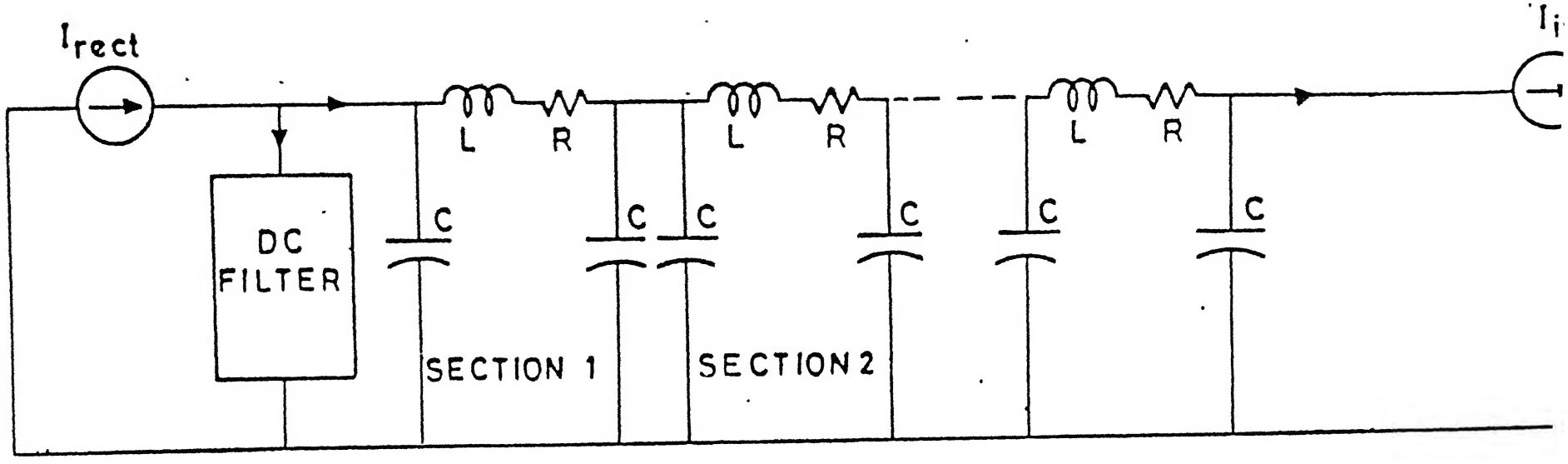


FIG. 4.2 DC LINE AND FILTER REPRESENTATION

$$V_c = K_1.(I_d - I_{ref})$$

Arrillaga [17], however, has suggested that the inclusion of a derivative term in the calculation of control voltage improves the dynamic behaviour of the system. Then the control signal V_c becomes

$$V_c = K_1.(I_d - I_{ref}) + K_2(dI_d/dt)$$

This control signal V_c is sampled at an appropriate time and this sampled value forms the basis for the calculation of Q_i.

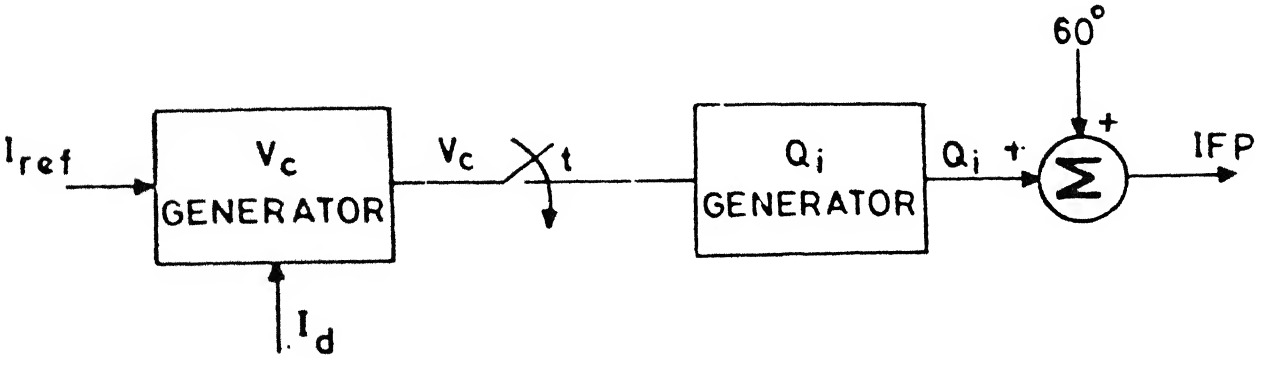


FIG. 4.3 CONVERTER CONSTANT CURRENT CONTROL

The other control at rectifier end is minimum firing angle control. In this control, the implementation technique is to calculate the voltage across the valve corresponding to the minimum firing angle and if at the instant of firing, the voltage across valve is less than this voltage, the valve conduction is prevented till the voltage rises to the rquired level. The transition between minimun firing angle control and constant current control is thus automatic [20].

4.5 INVERTER END CONTROLS

The thyristor inverter control was constant extinction angle control and constant current control. Under normal conditions, the operation was in constant extinction angle control mode. Since GTO thyristor is used at inverter end and there is no cocept like extinction angle because of the facility of extinction of GTO valve at any desired instant. The firing time and extinction time of a GTO converter is decided by modulation index which can be varried between 0 and 1. Since regeneration time is required for normal operation so the value of modulation index is limited between 0.05 to 0.95. In this thesis, EPWM scheme with 12 voltage pulses per ac cycle is used. The firing and extinction instants of GTOs are calculated by expression given in table (2.1).

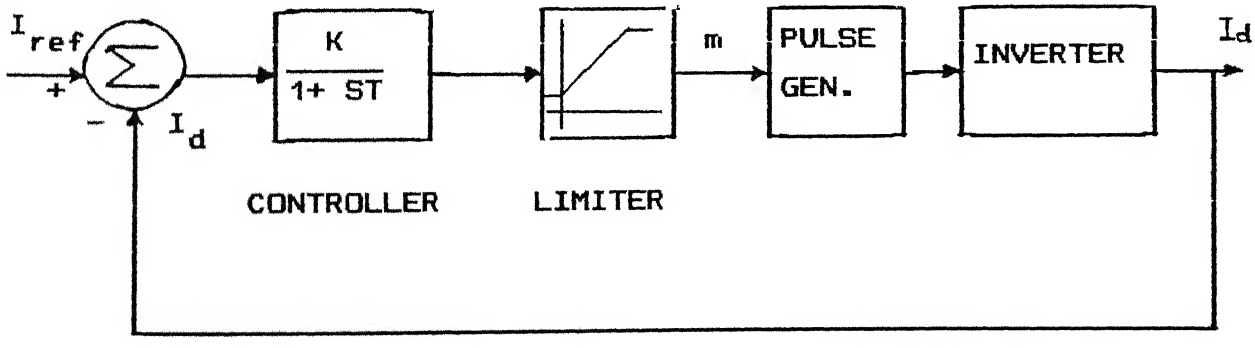


FIG. 4.4 BLOCK DIAGRAM OF INVERTER CURRENT CONTROL

Basically there are three terms in the expression (I.4) of Appendix I (i.e. dc voltage, dc current & modulation index).

Therefore one can control any of them or two of them simultaneously or even all of them. Since conventional thyristor inverters have constant current control and constant extinction angle control(CEA). In the same way here performance study is tried for GTO inverter using one of the following two alternatives. They are :

1. constant current control and constant dc VOLTAGE ~~extinction angle~~ control

2. constant current control and constant modulation index control.

In PWM GTO converter, two modes of operation is performed, one is power mode in which ac source is directly connected to the dc system and other is freewheeling mode in which ac source is disconnected and there is dc short circuit. Due to large variation in dc voltage, the use of constant voltage control is very difficult, however, voltage transducer may be used to solve this problem but it will increase the system time constant. In this thesis, the study of the GTO inverter control is performed on the constant current control and constant modulation index. Constant modulation control is similar to the CEA control of thyristor inverter. In order to avoid the operation of both rectifier end current controller and inverter end current controller, a margin of 10% in current refference is given. When the inverter dc current decreases below 0.9 p.u., the current controller of inverter end starts working and for other cases

modulation index control. The value of margin is so chosen that the transition beween inverter end controller is smooth. The output of constant current controller is directly related to the modulation index and firing & extinction angles are calculated at every instants. The block diagram of constant current control of inverter has been given in Figure (4.4).

4.6 COMPUTER PROGRAM

The development of a digital computer program for simulating an HVDC system with thyristor rectifier and inverter is described in reference [17]. This incorporates both 6 and 12 pulse converter representation along with firing control schemes based on IPC and EPC. The program is extremely modular and therefore permits implementation of different control schemes and other advance features necessary to simulate a practical system. The program is augmented by Ajai [20] to include digital control scheme, dc filters and dc line faults. This program is further augmented to replace thyristor inverter by GTO inverter. Suitable control schemes are incorporated for the simulation of an HVDC system with GTO inverter. The basic flow chart is same as in reference[20]. The computation of modulation index from controller output, hence firing and extinction instant of GTO valves are calculated to check the incoming and outgoing GTOs. The program which was augmented and reported in reference [20] is used suitably with some modification for GTO inverter in place of thyristor inverter.

The simulation can start either assuming the system under steady state operating condition or with initial condition. In the case of former the initial conditions for various state variables have to be supplied. The calculation of initial conditions for all state variables except for GTO inverter variables have been reported in reference [20]. The initial conditions for GTO inverter state variables are calculated in chapter 3.

4.7 CASE STUDY

The effect of GTO inverter in HVDC system is investigated in detail by digital simulation. The operating conditions and parameters are given in Appendix VI which is taken from reference [20]. The control parameters for GTO inverter are also included. The detail investigation includes the comparision of rectifier / inverter dc voltage and current with thyristor rectifier / inverter, harmonic analysis and reactive power requirement.

4.7.1 Steady State Simulation

To demonstrate the program capability, steady state performance of HVDC system with six pulse converter configuration at rectifier end and GTO converter at inverter end has been studied. Figures (4.5) to (4.8) are the instanteneous plots of rectifier dc voltage, dc current, inverter dc voltage and dc current respectively. The average value of rectifier dc voltage and dc current, inverter dc voltage and dc current are given in

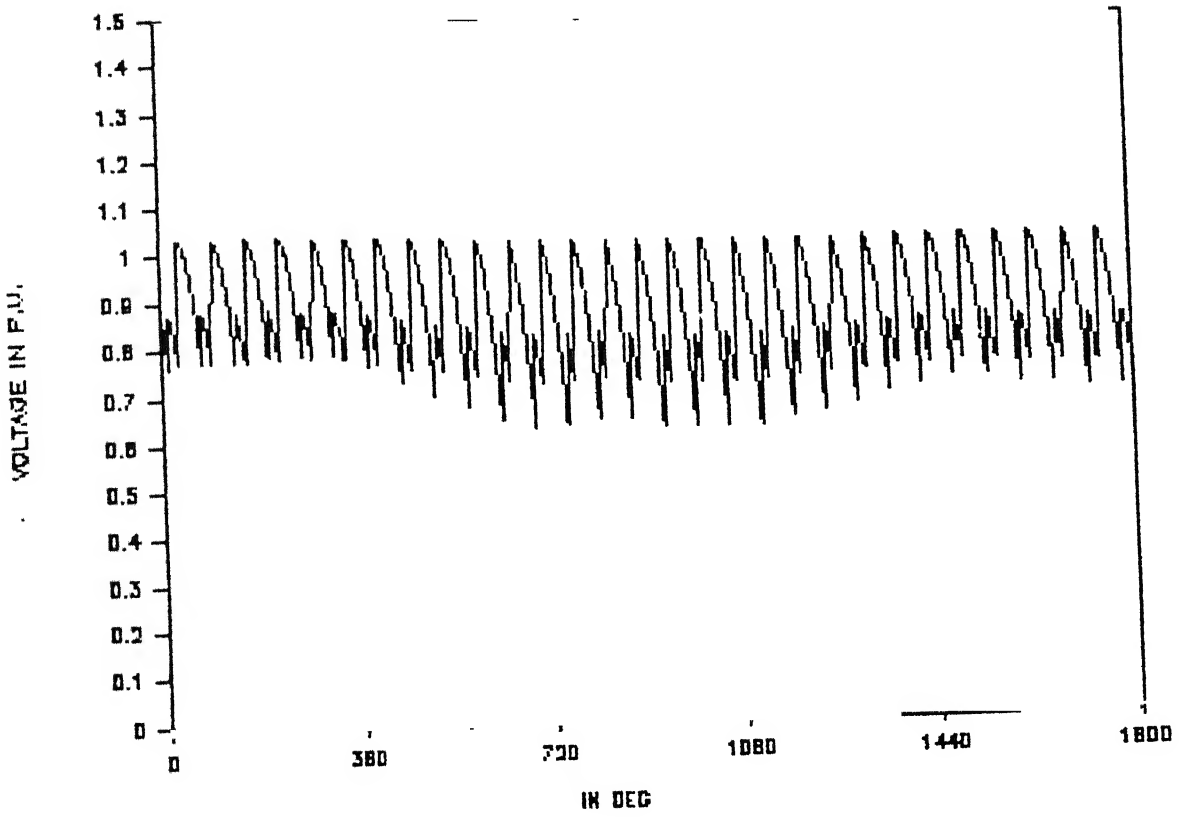
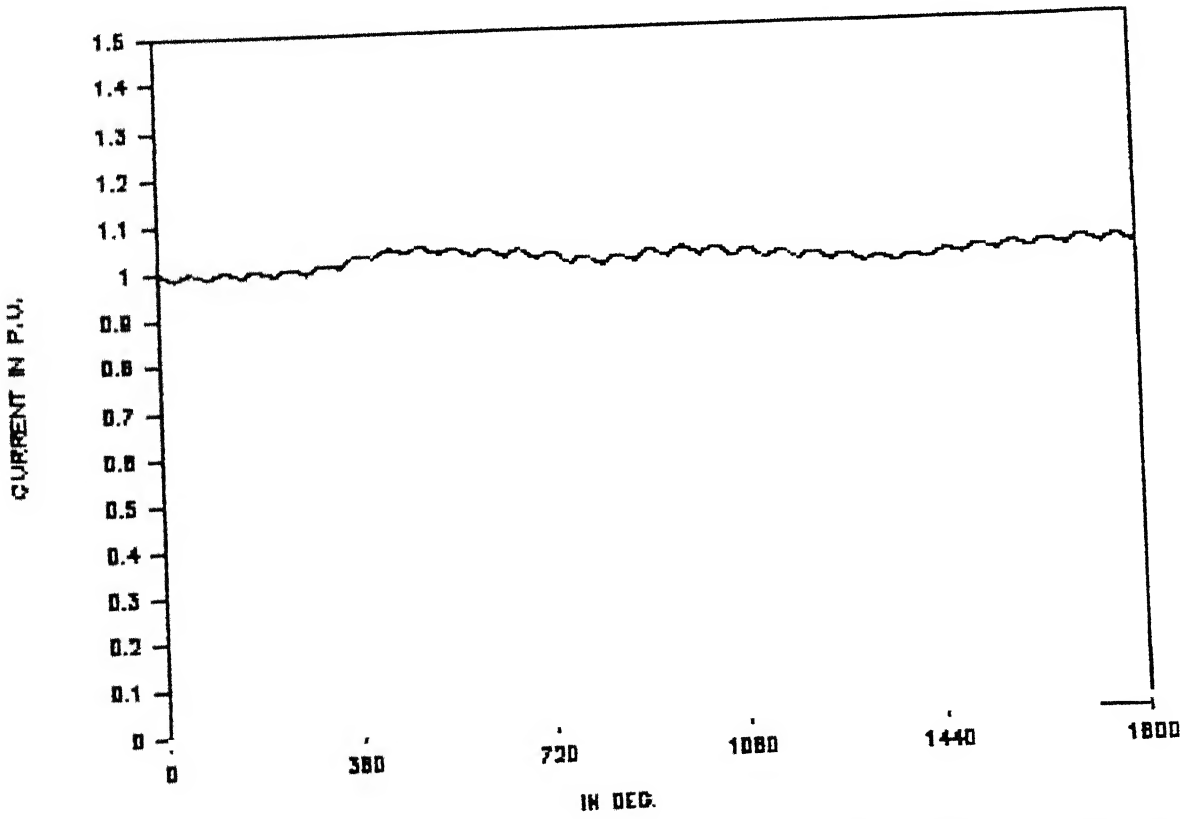


FIG. 4.5 RECTIFIER INSTANTENEOUS DC VOLTAGE UNDER STEADY STATE



RECTIFIER INSTANTENEOUS DC CURRENT UNDER STEADY STATE

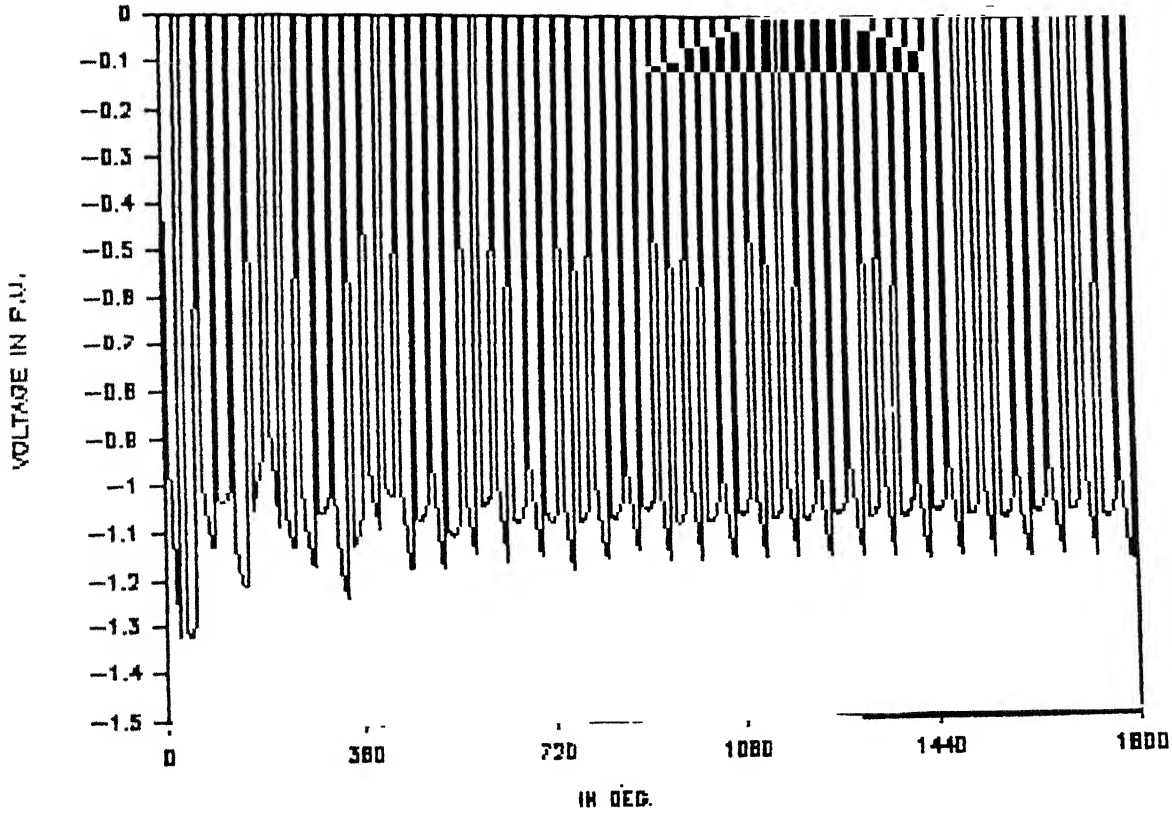


FIG. 4.7 INVERTER INSTANTENEOUS DC VOLTAGE UNDER STEADY STATE

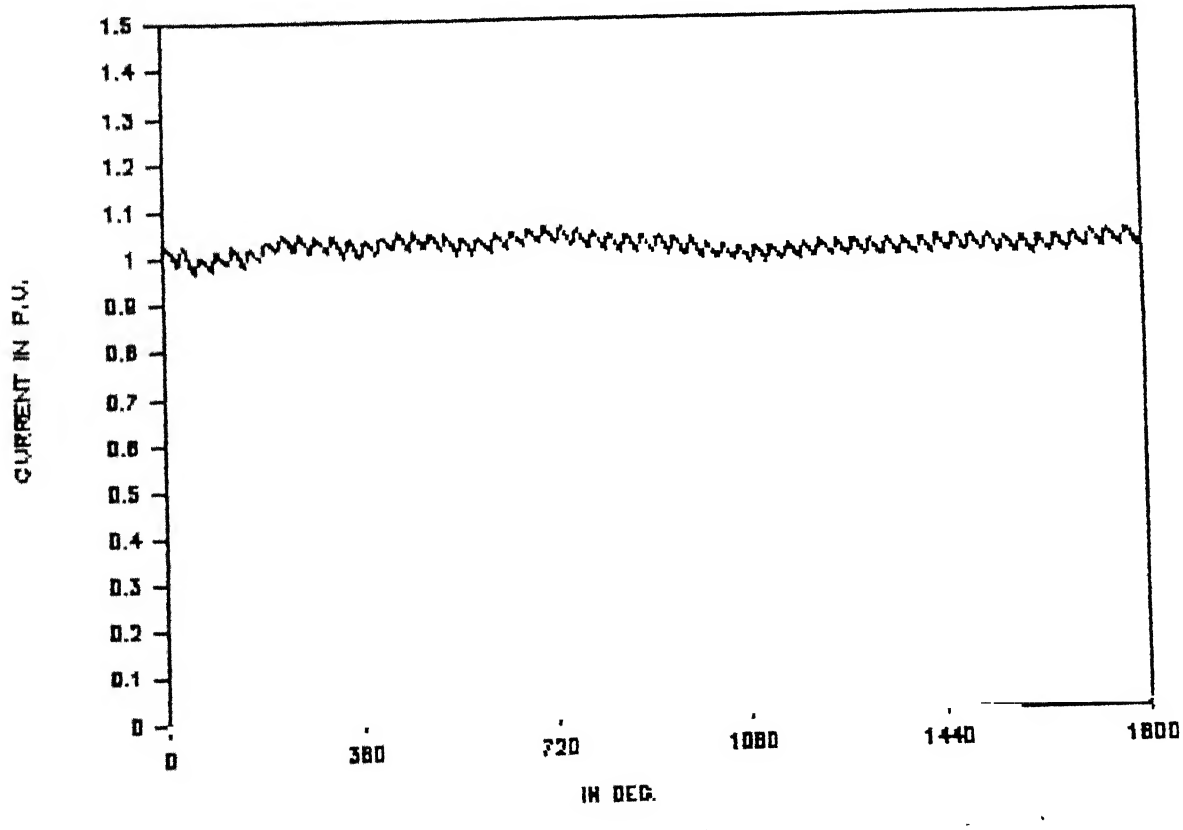


FIG. 4.8 INVERTER INSTANTENEOUS DC CURRENT UNDER STEADY ST

Figures (4.9)to (4.12). The harmonic components of ac and dc sides of inverter end are shown in Figures (4.13) to (4.16). The ac current in a phase and ac voltage are given in Figure (4.17) to show the power factor. The harmonics and power factor of thyristor inverter are well known [1].

4.7.2 Transient Response

The dynamical behaviour of the HVDC system employing 6 pulse thyristor rectifier and GTO inverter has been investigated with current reference change and ac voltage dip on the both sides of converter. The average dc voltage and average dc current at both rectifier and inverter end, harmonic components of ac and dc values (voltage/current) of inverter end during fault(1st cycle) are plotted. The following cases are studied.

Case No.	Name of case
1.	Change in current reference by 20%
2.	99% dip in one phase for 10 cycle at rectifier end
3.	99% dip in two phases for 5 cycle at rectifier end
4.	50% dip in all phases for 5 cycle at rectifier end
5.	99% dip in one phase for 10 cycle at inverter end
6.	99% dip in two phases for 5 cycle at inverter end
7.	99% dip in all phases for 5 cycle at inverter end
8.	50% dip in all phases for 5 cycle at inverter end

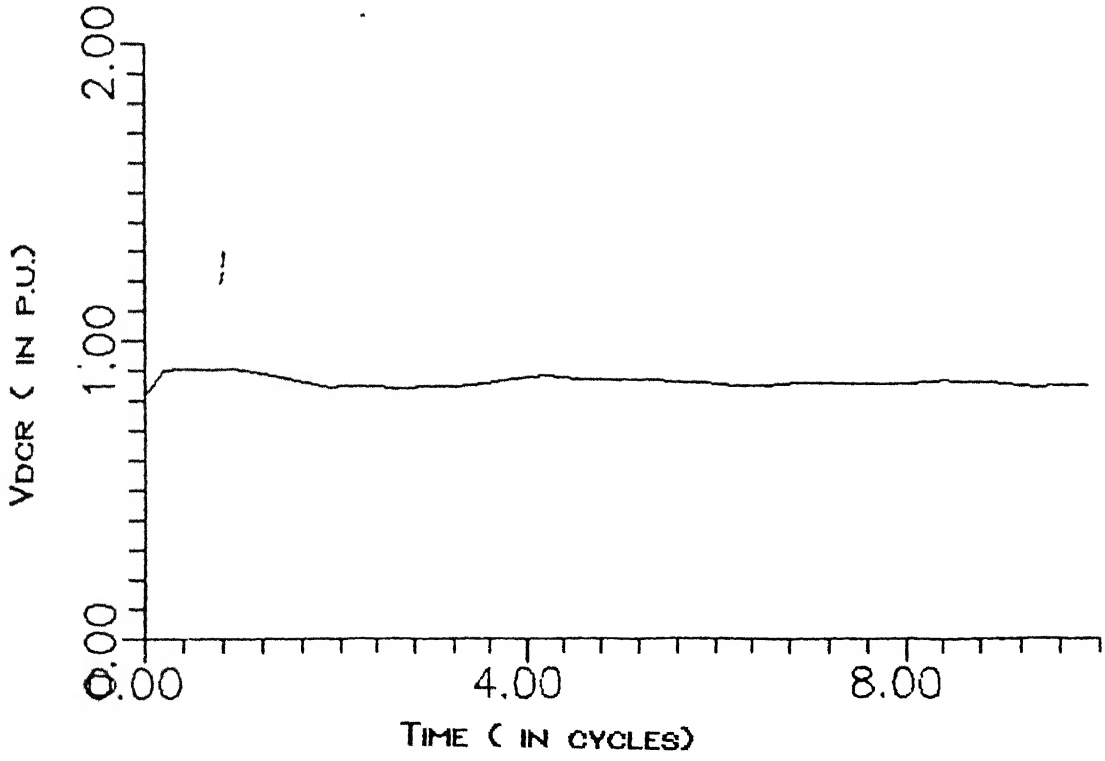


FIG. 4.9 RECTIFIER AVERAGE DC VOLTAGE UNDER STEADY STATE

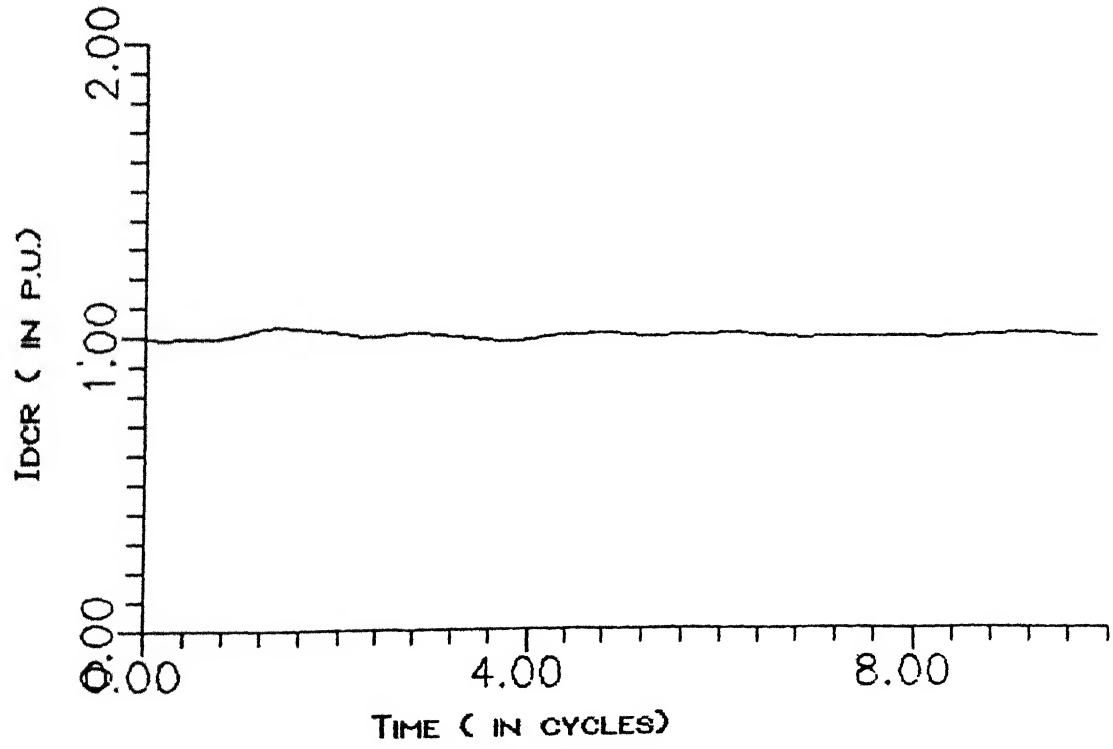


FIG. 4.10 RECTIFIER AVERAGE DC CURRENT UNDER STEADY STATE

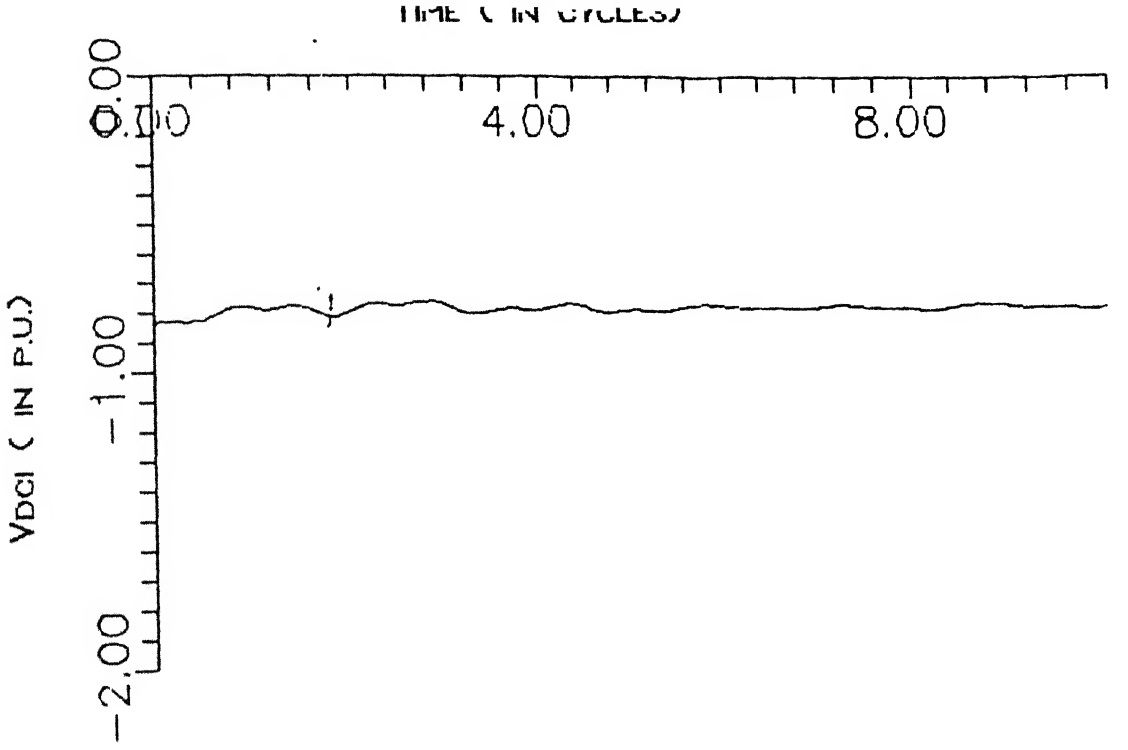


FIG. 4.11 INVERTER AVERAGE DC VOLTAGE UNDER STEADY STATE

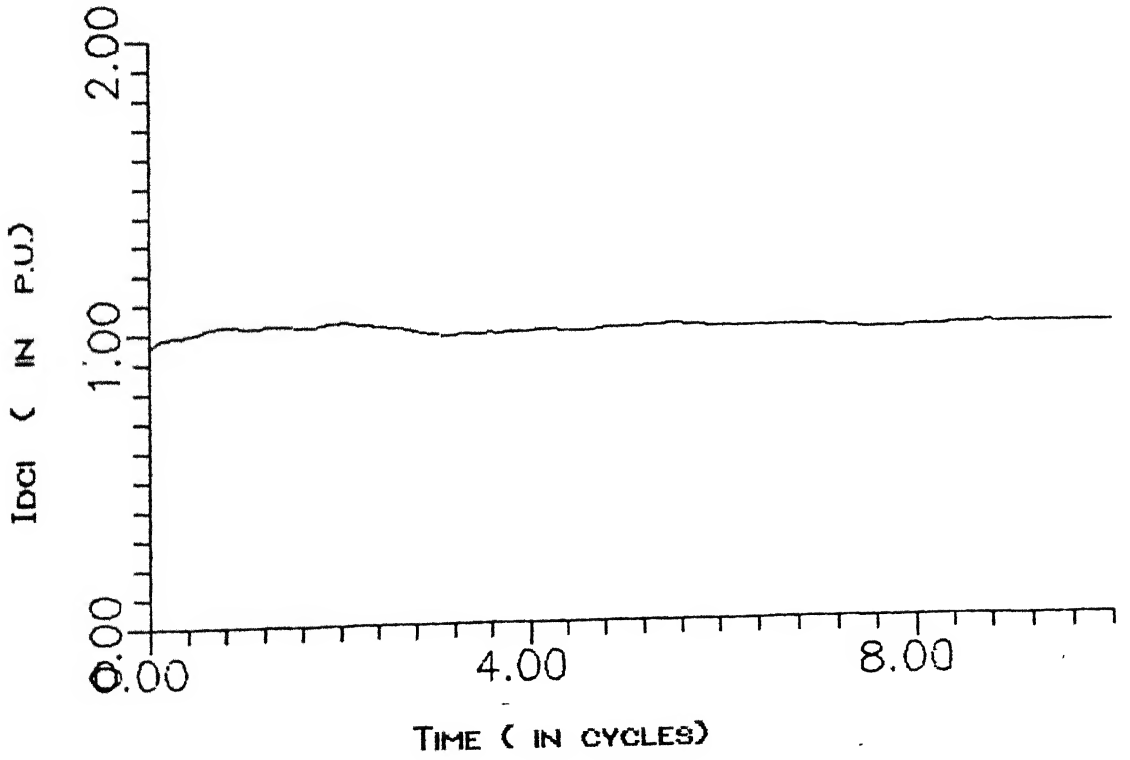


FIG. 4.12 INVERTER AVERAGE DC CURRENT UNDER STEADY STATE

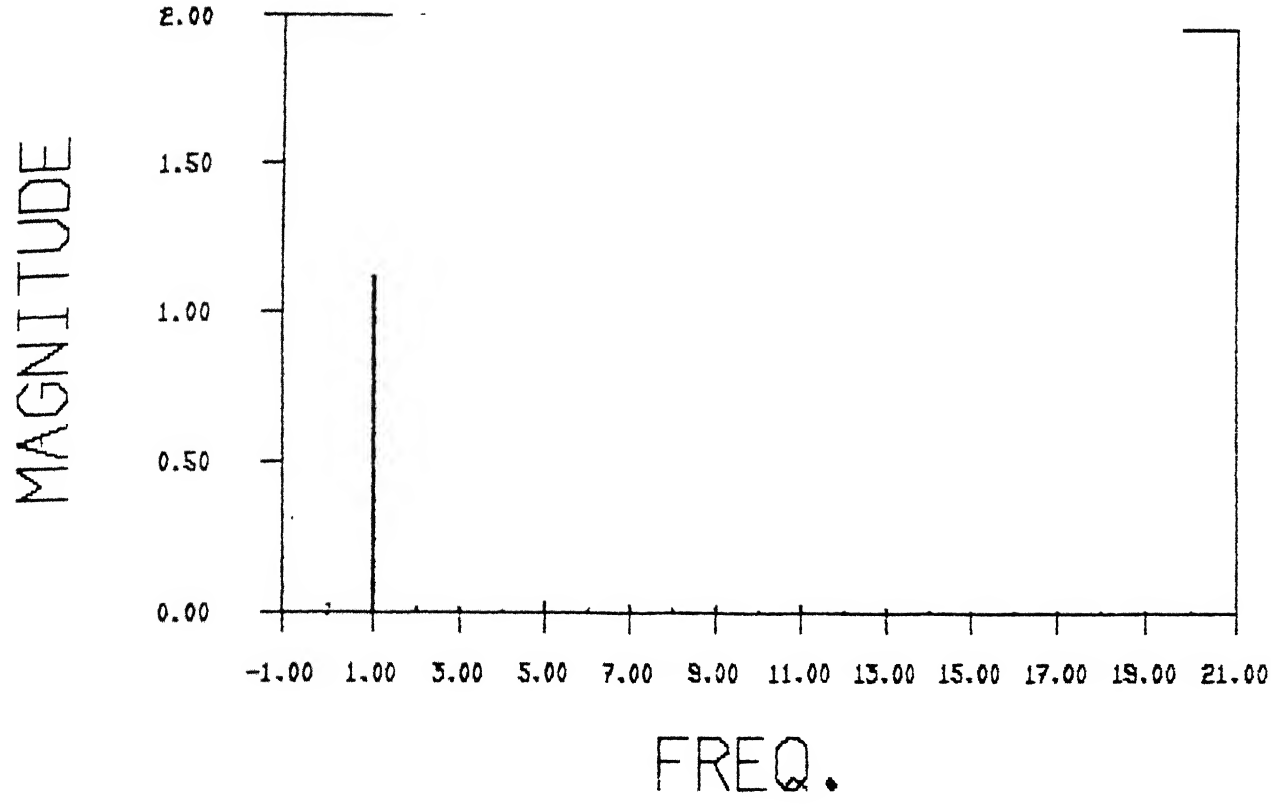


FIG. 4.13 HARMONIC COMPONENTS OF INVERTER AC VOLTAGE

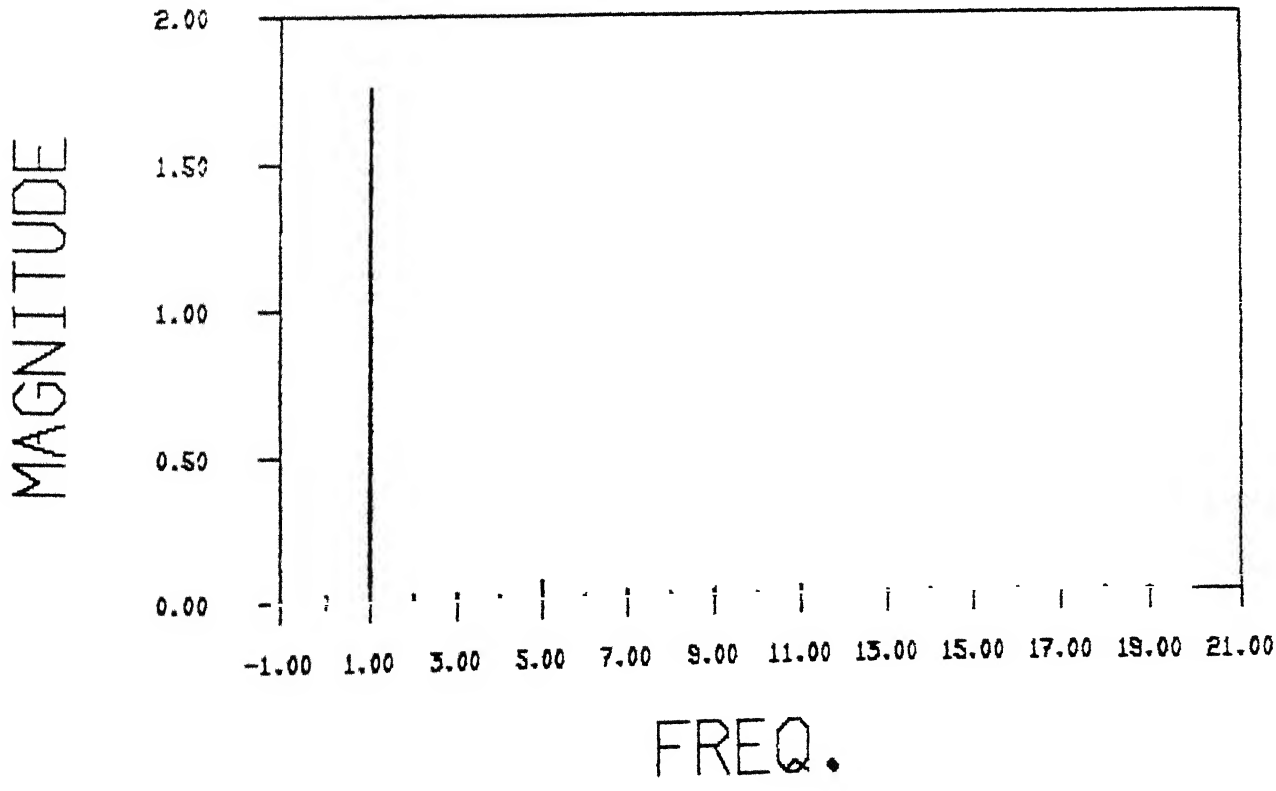


FIG. 4.14 HARMONIC COMPONENTS OF INVERTER AC CURRENT

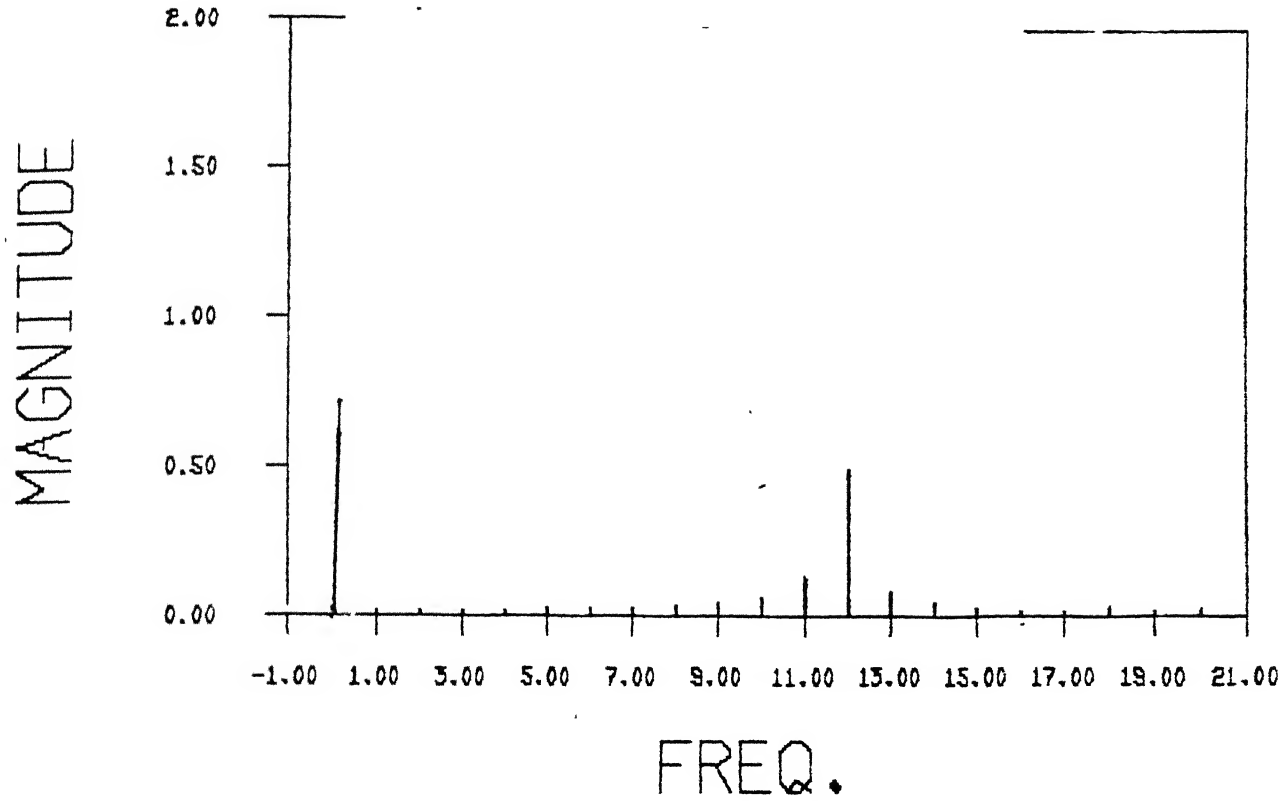


FIG. 4.15 HARMONIC COMPONENTS OF INVERTER DC VOLTAGE

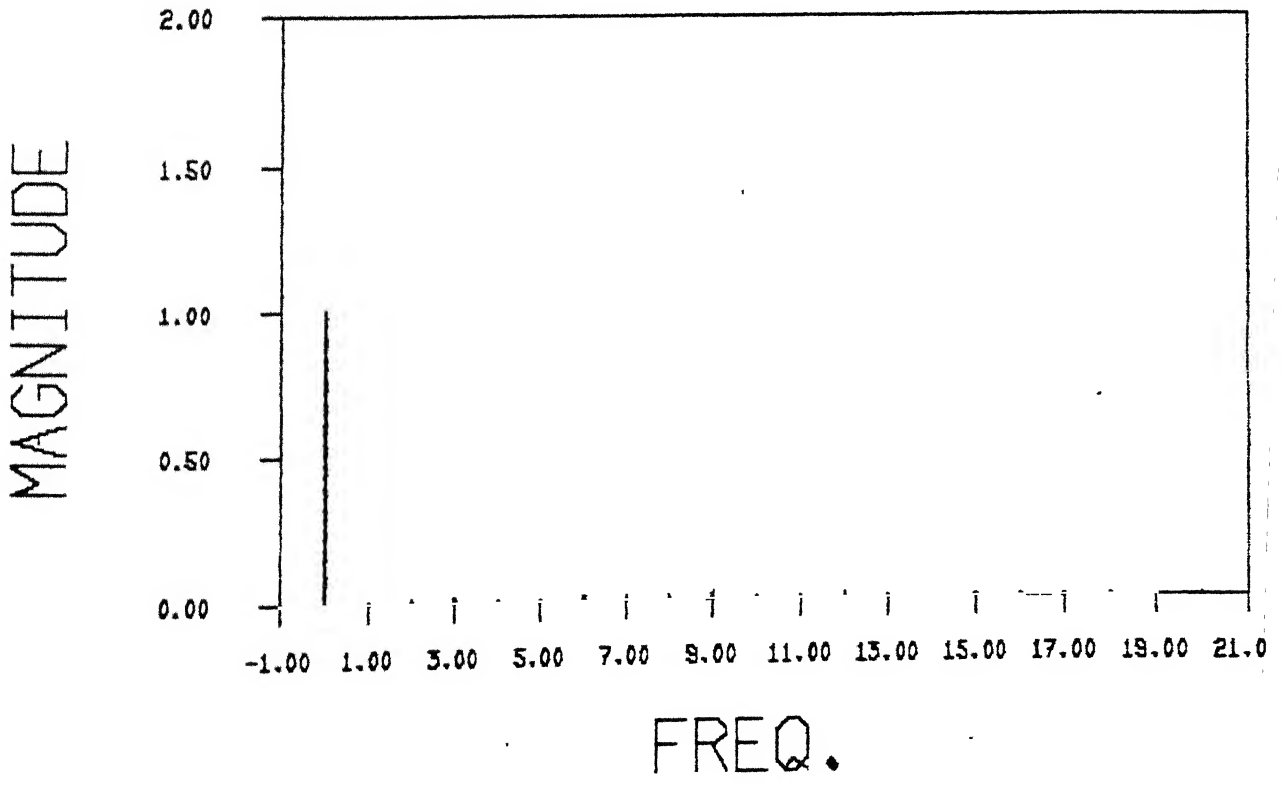


FIG. 4.16 HARMONIC COMPONENTS OF INVERTER DC CURRENT

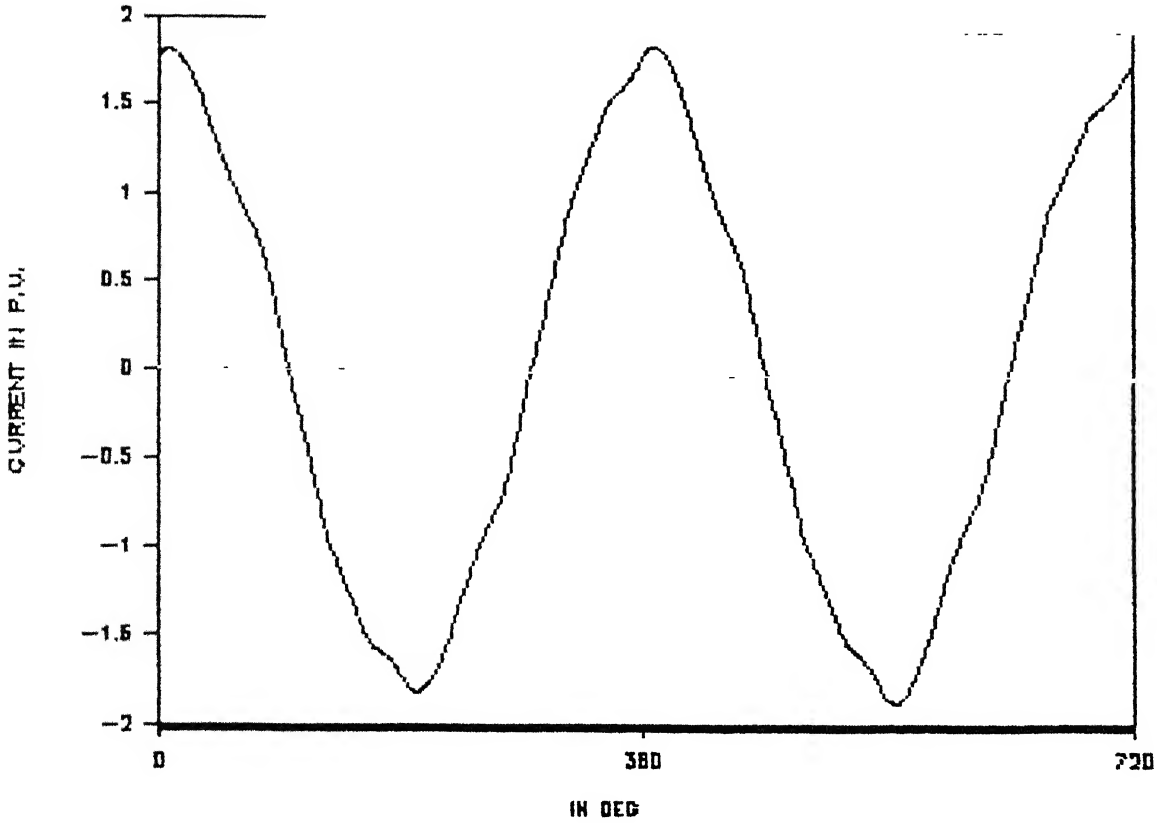


FIG. 4.17(a) INVERTER PHASE 'C' CURRENT

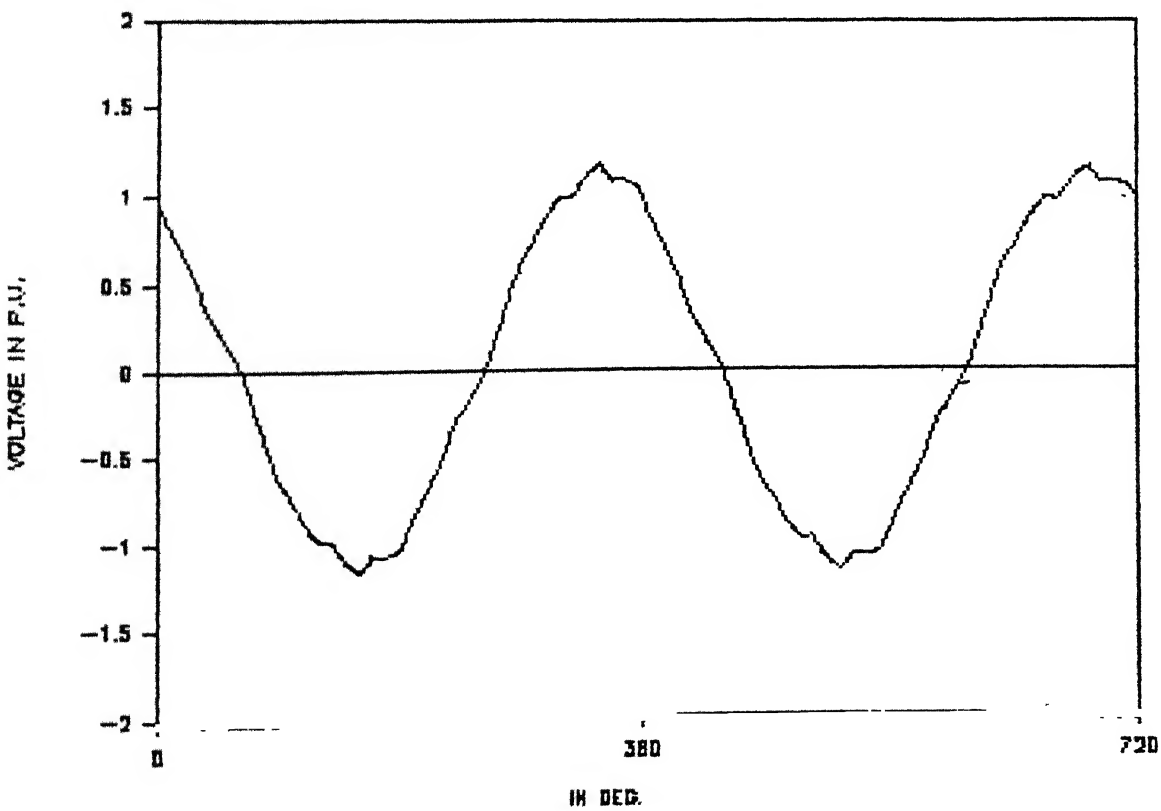


FIG. 4.17(b) INVERTER PHASE C-B VOLTAGE

(1) Change in Current Reference:

The response for two terminal case shows that the current controller at rectifier end comes into action as a step change in the current refernce is applied to the both ends. The inverter current controller will work only when dc current will fall down below set the value. The application of reference change, the current settles down to the new value in certain time which is dependent on gain and time constant of controllers. Figure (4.18) shows the rectifier end average voltage and current following 20% increase in current reference at both ends of the converter. The inverter end average dc voltage and dc current are shown in Figures (4.19) & (4.20) respectively.

(2). 99% dip in one phase at rectifier:

The probability of this fault is very high but severety is low. Figures (4.21) &(4.22) show the average dc voltage and dc current at rectifier end, and inverter end average dc voltage and current are given in Figures (4.23) & (4.24) respectively. The harmonic components of inverter end ac voltage,ac current, dc voltage, dc current are given in Figures (4.25) to (4.28) respectively. The power factor can be seen by Figures (4.29) and (4.30).

(3) 99% dip in two phases at rectifier :

The dip of 99% is provided in phases 'A' & 'B' for 5 cycle at the begining of 5th cycle. The average dc voltage and current of rectifier terminal are shown in Figures (4.31) &

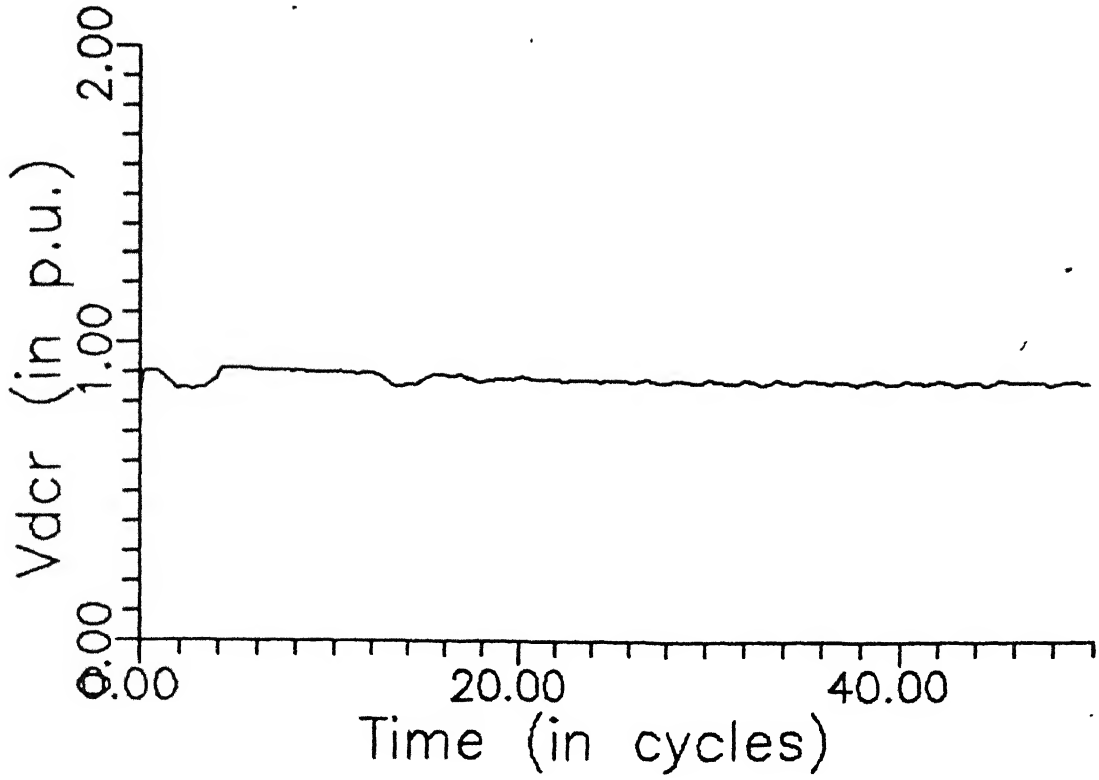


FIG. 4.18(a) RECTIFIER TERMINAL DC VOLTAGE FOR CASE 1

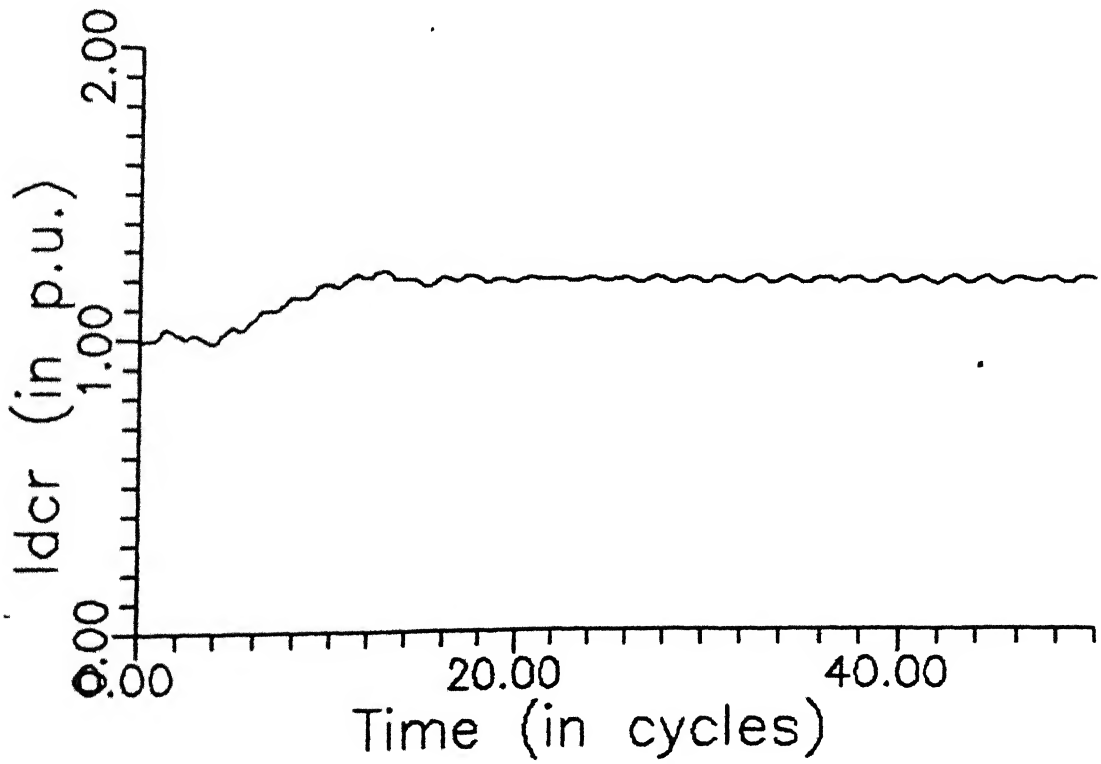


FIG. 4.18(b) RECTIFIER TERMINAL DC CURRENT FOR CASE 1

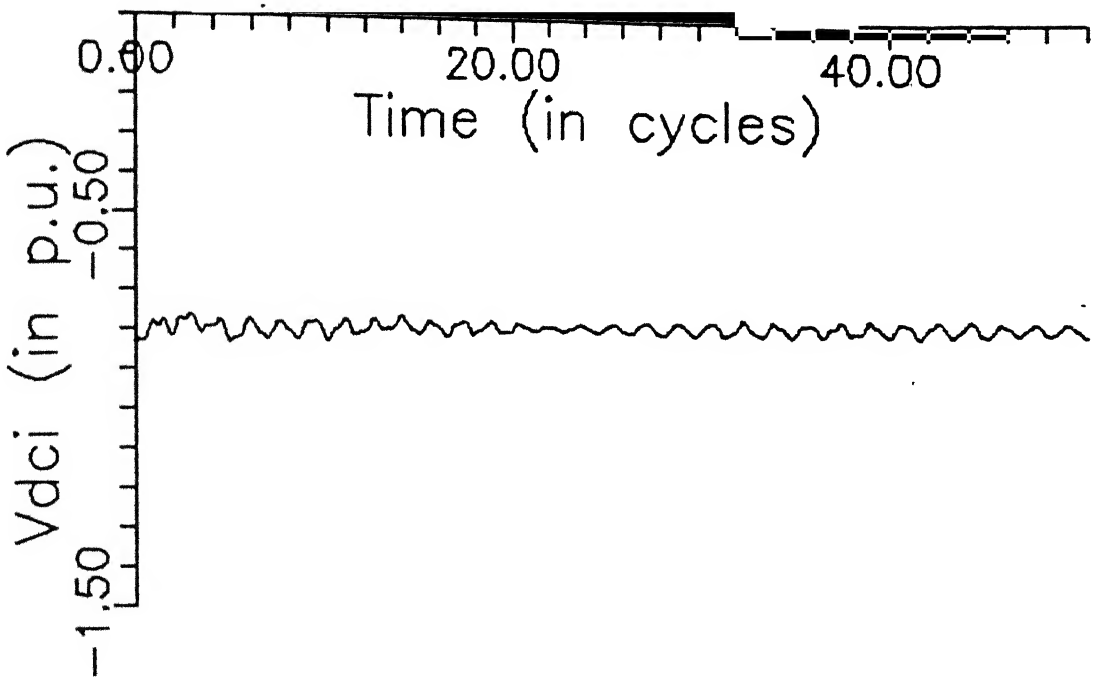


FIG. 4.19 INVERTER TERMINAL DC VOLTAGE FOR CASE 1

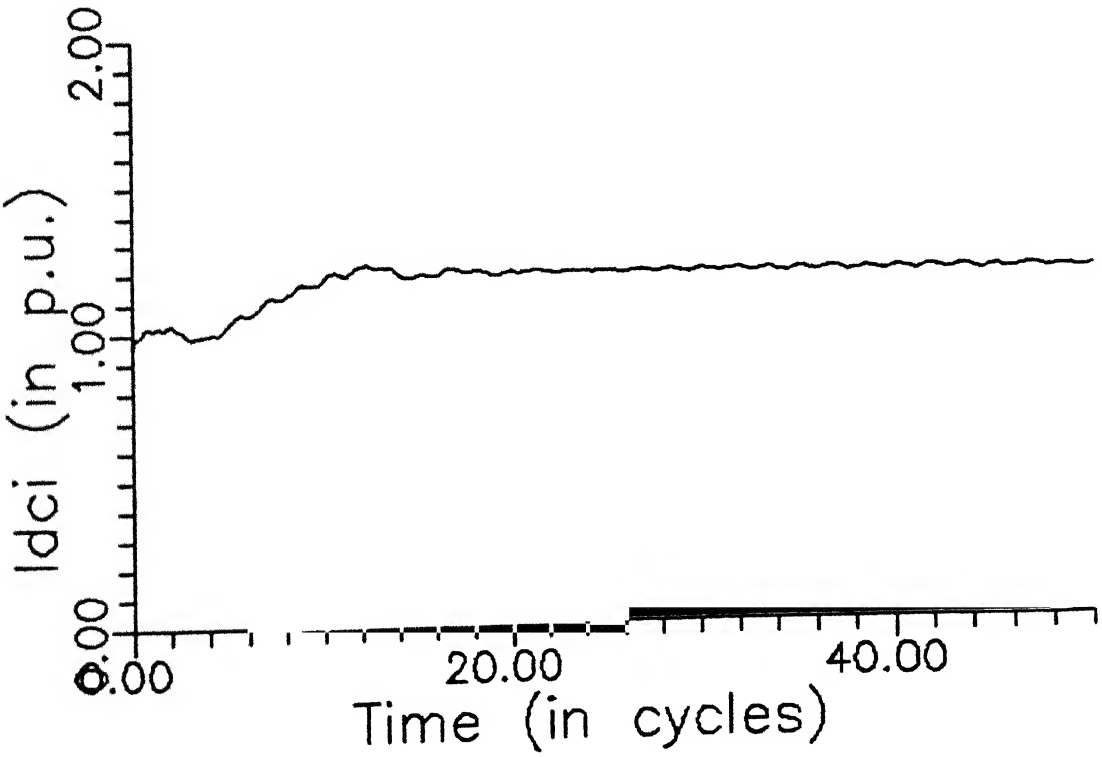


FIG. 4.20 INVERTER TERMINAL DC CURRENT FOR CASE 1

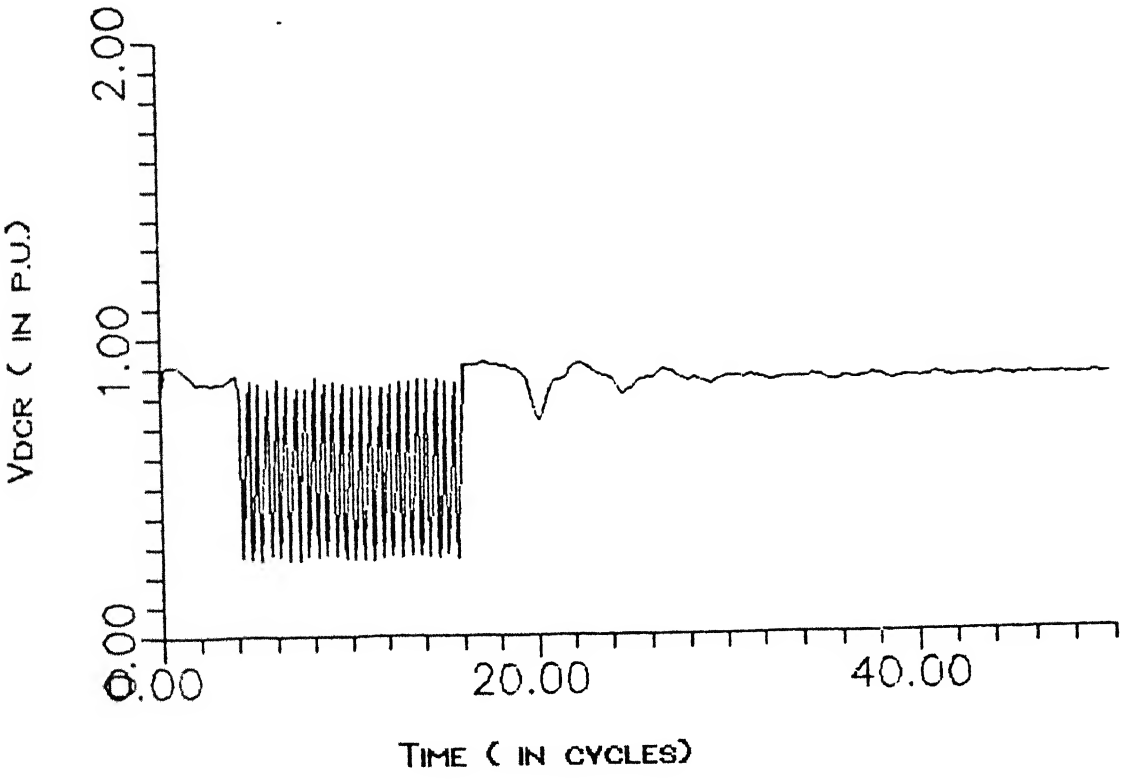


FIG. 4.21 RECTIFIER TERMINAL DC VOLTAGE FOR CASE 2

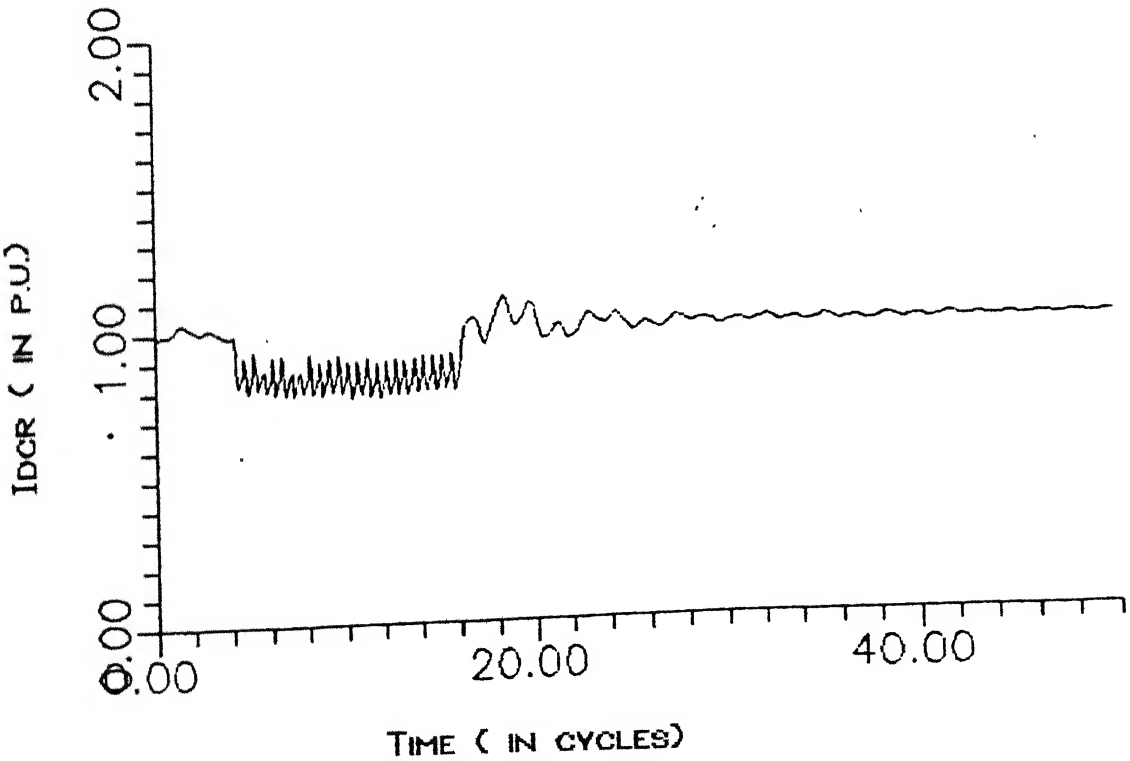


FIG. 4.22 RECTIFIER TERMINAL DC CURRENT FOR CASE 2

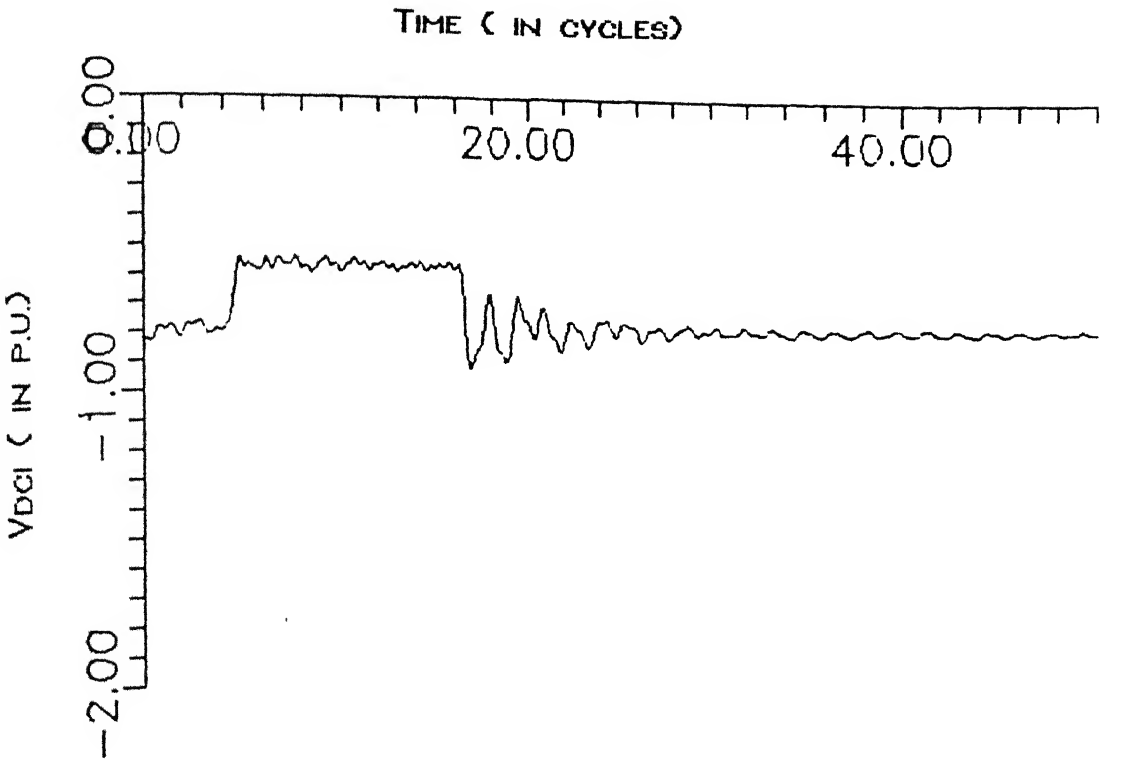


FIG. 4.23 INVERTER TERMINAL DC VOLATGE FOR CASE 2

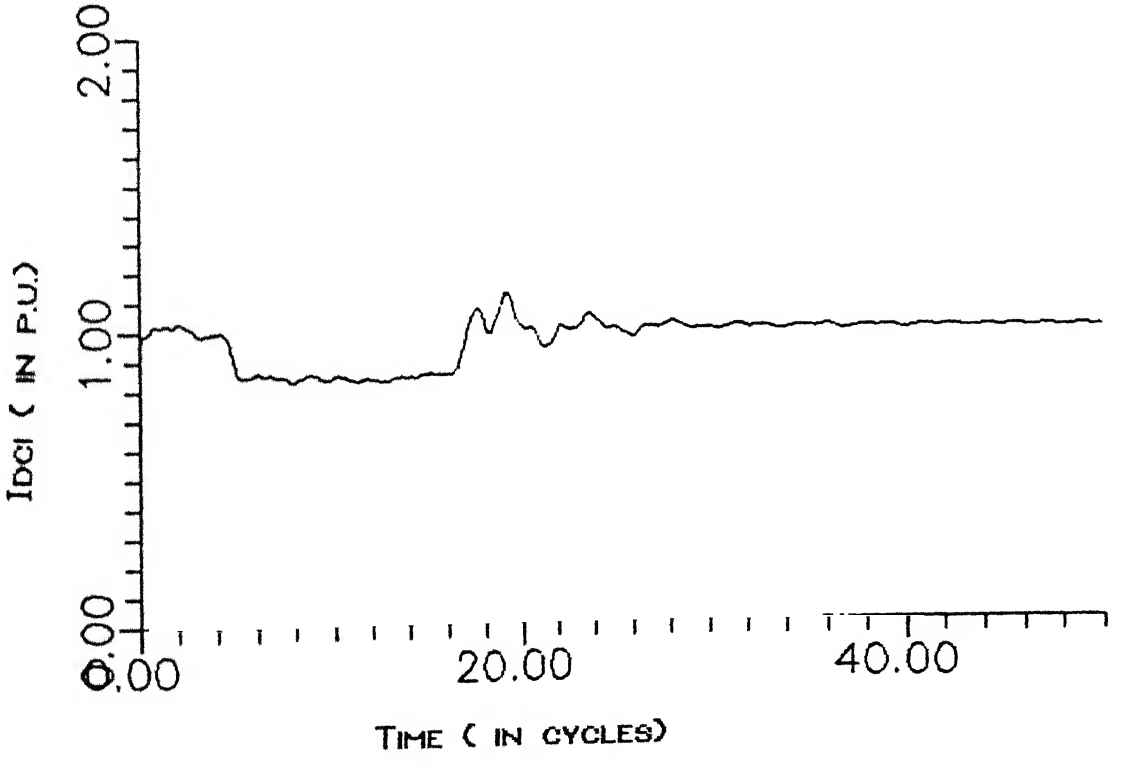


FIG. 4.24 INVERTER TERMINAL DC CURRENT FOR CASE 2

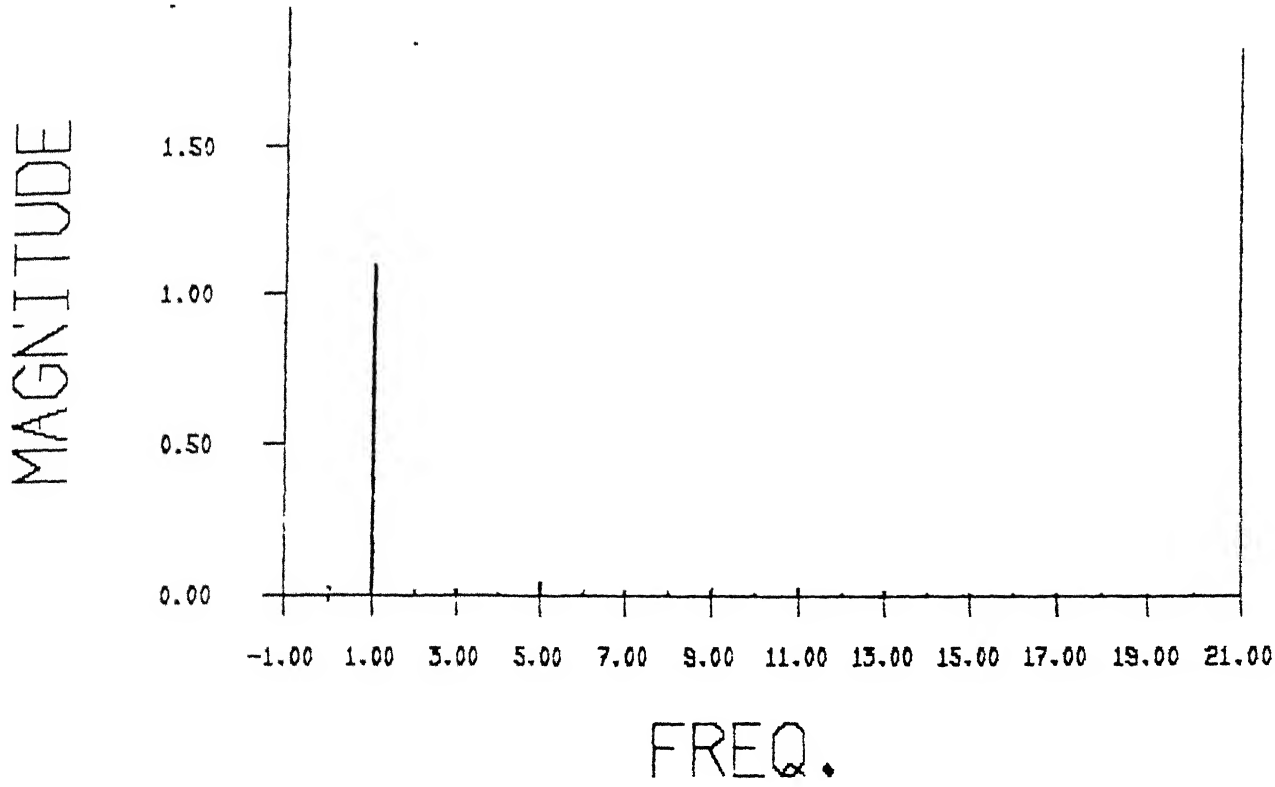


FIG. 4.25 HARMONIC COMPONENTS OF INVERTER AC VOLTAGE FOR CASE 2

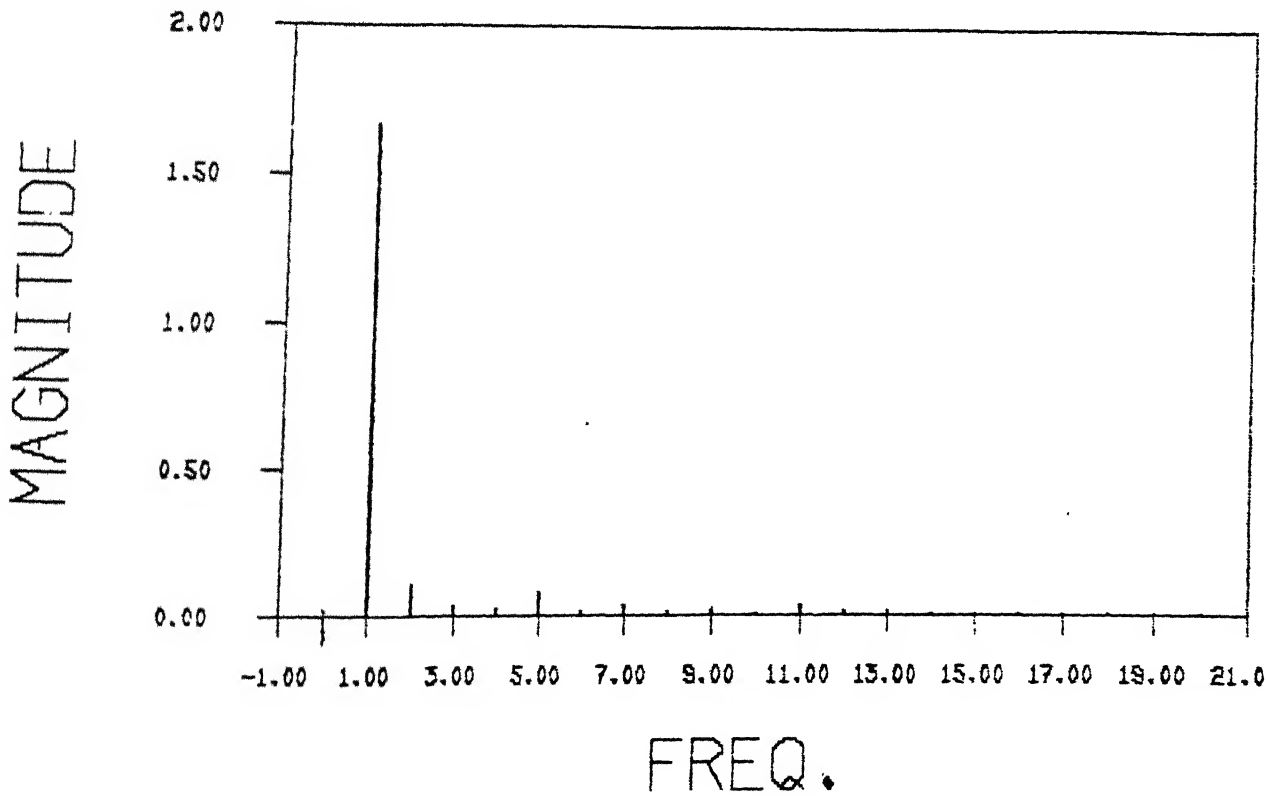


FIG. 4.26 HARMONIC COMPONENTS OF INVERTER AC CURRENT FOR CASE

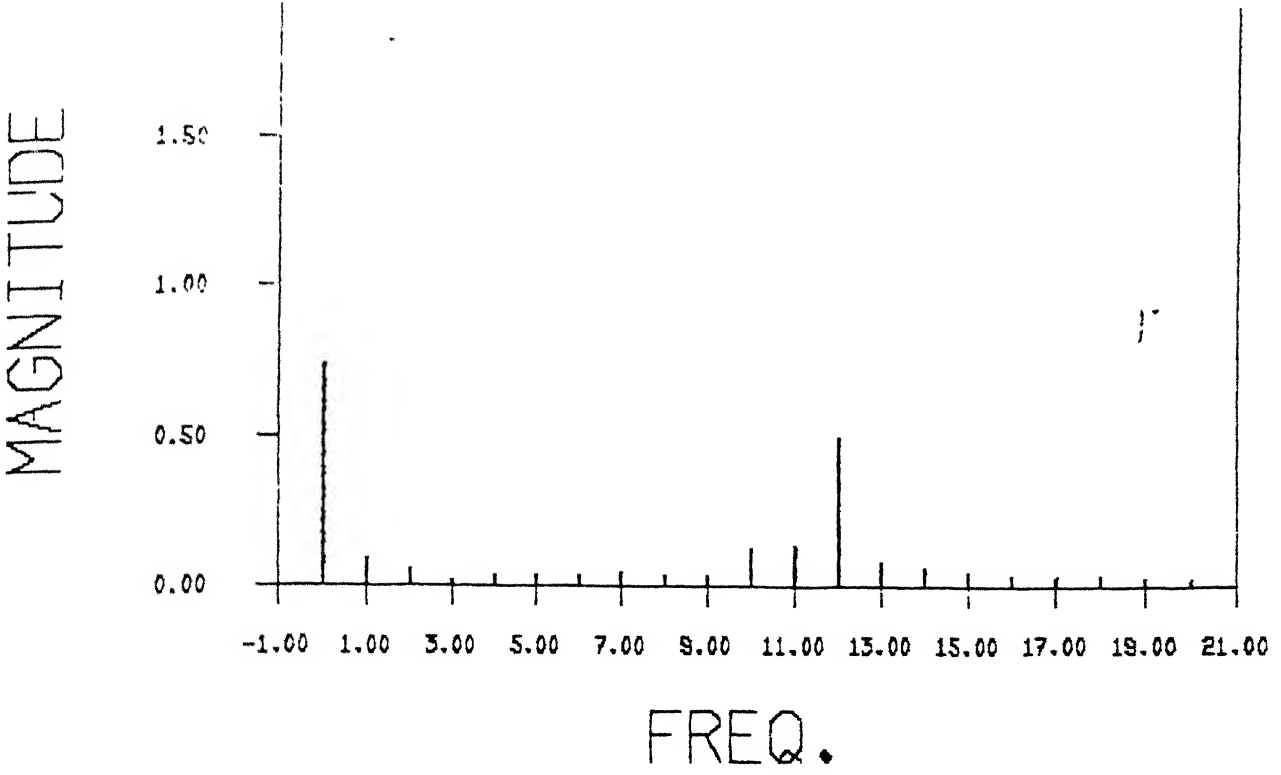


FIG. 4.27 HARMONIC COMPONENTS OF INVERTER DC VOLTAGE FOR CASE

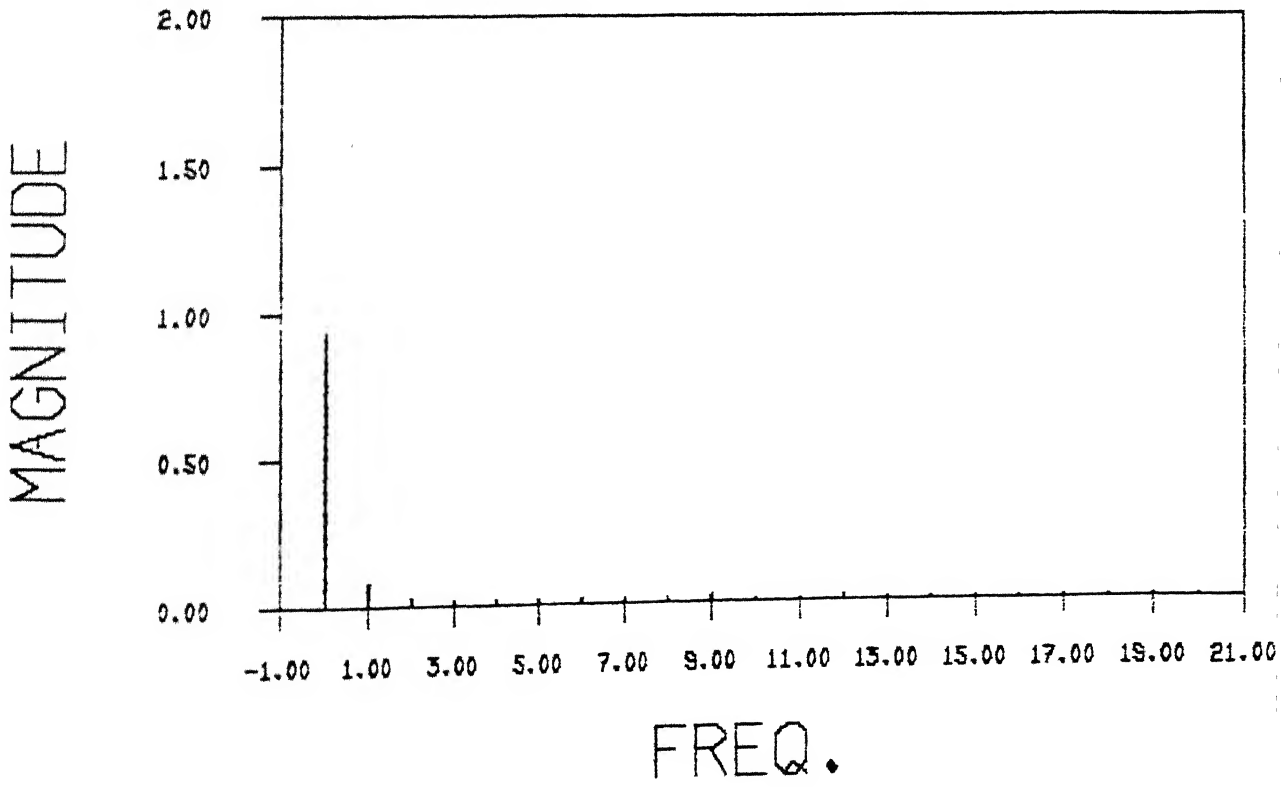


FIG. 4.28 HARMONIC COMPONENTS OF INVERTER DC CURRENT FOR CASE

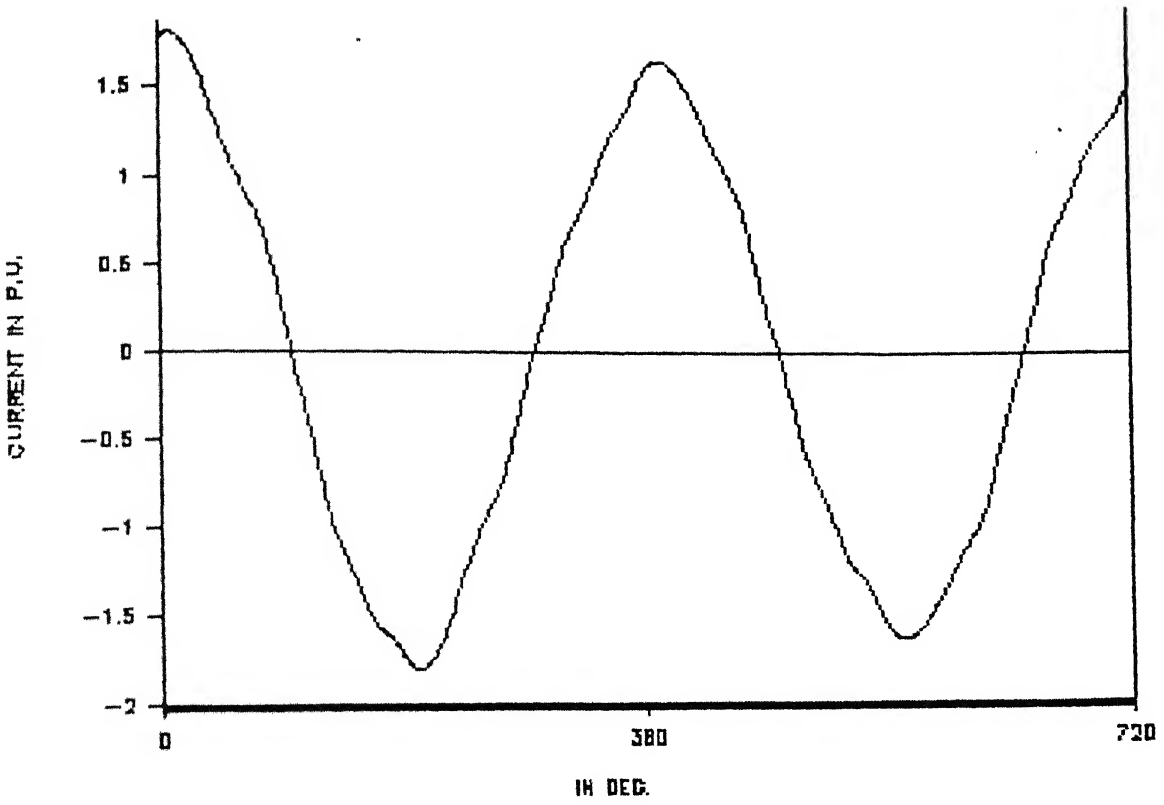


FIG. 4.29 INVERTER PHASE 'C' CURRENT FOR CASE 2

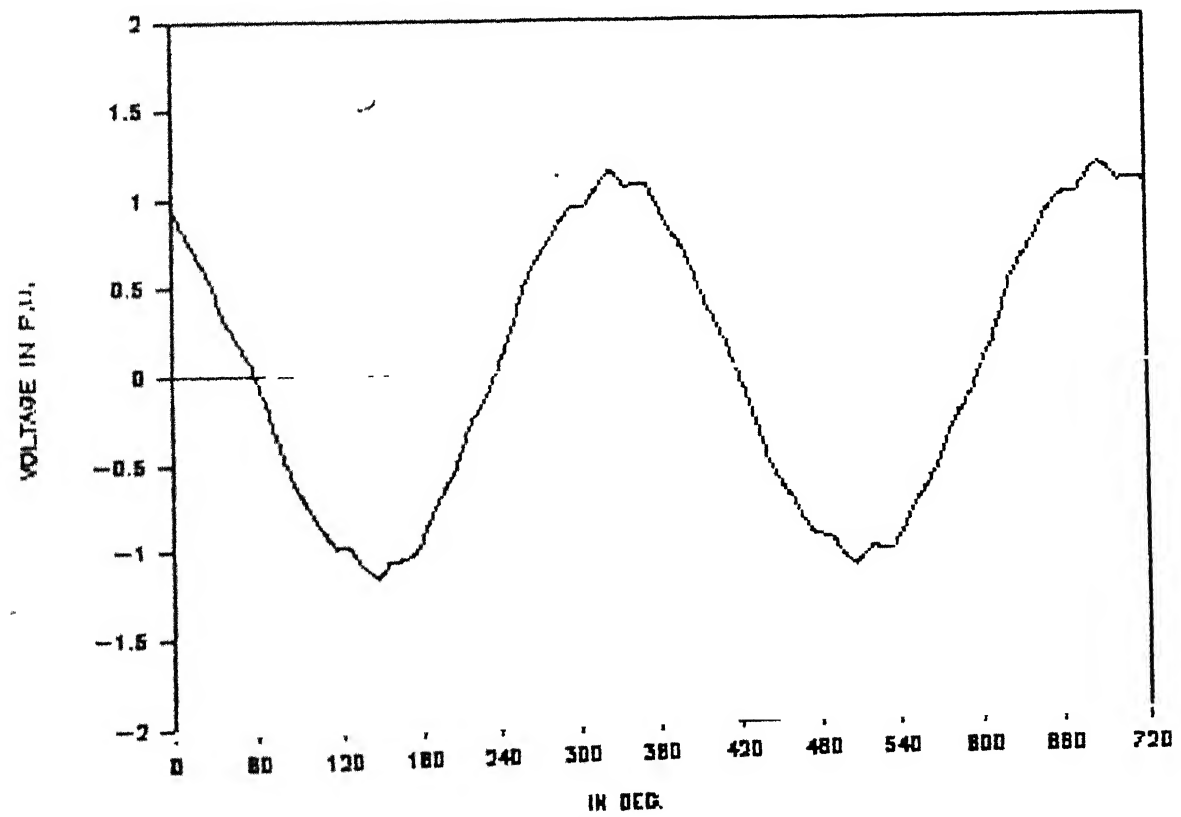


FIG. 4.30 INVERTER PHASE C-B VOLTAGE

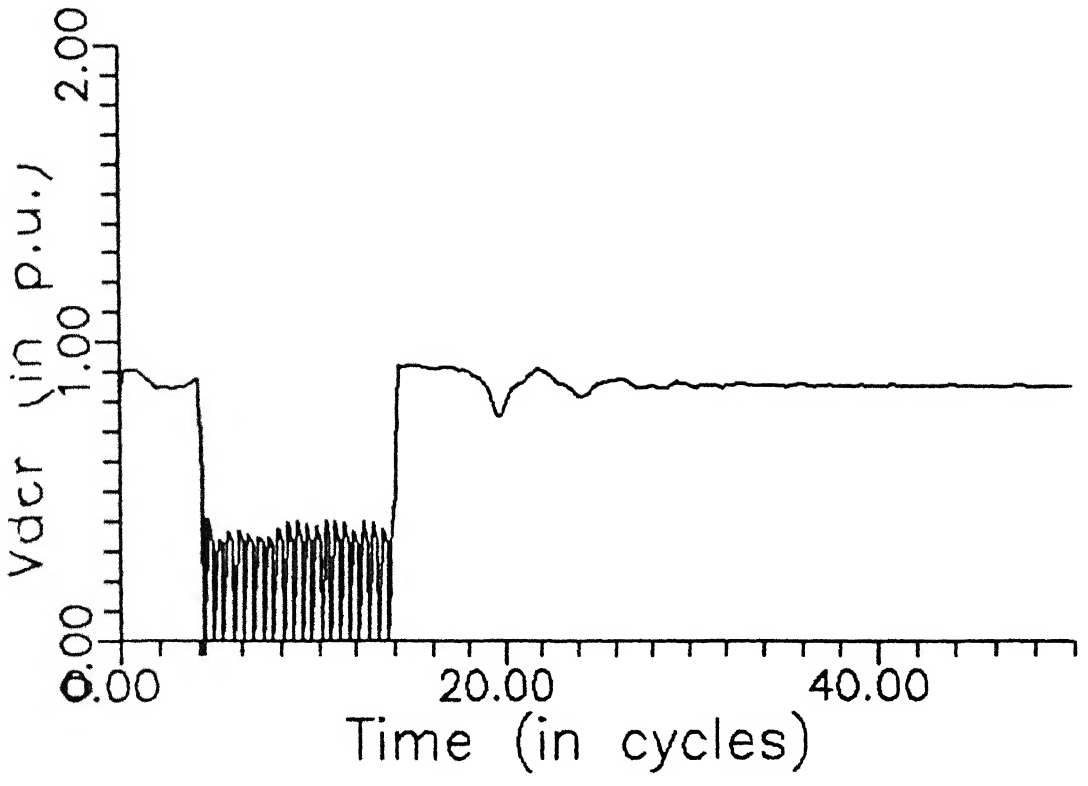


FIG. 4.31 RECTIFIER TERMINAL DC VOLTAGE FOR CASE 3

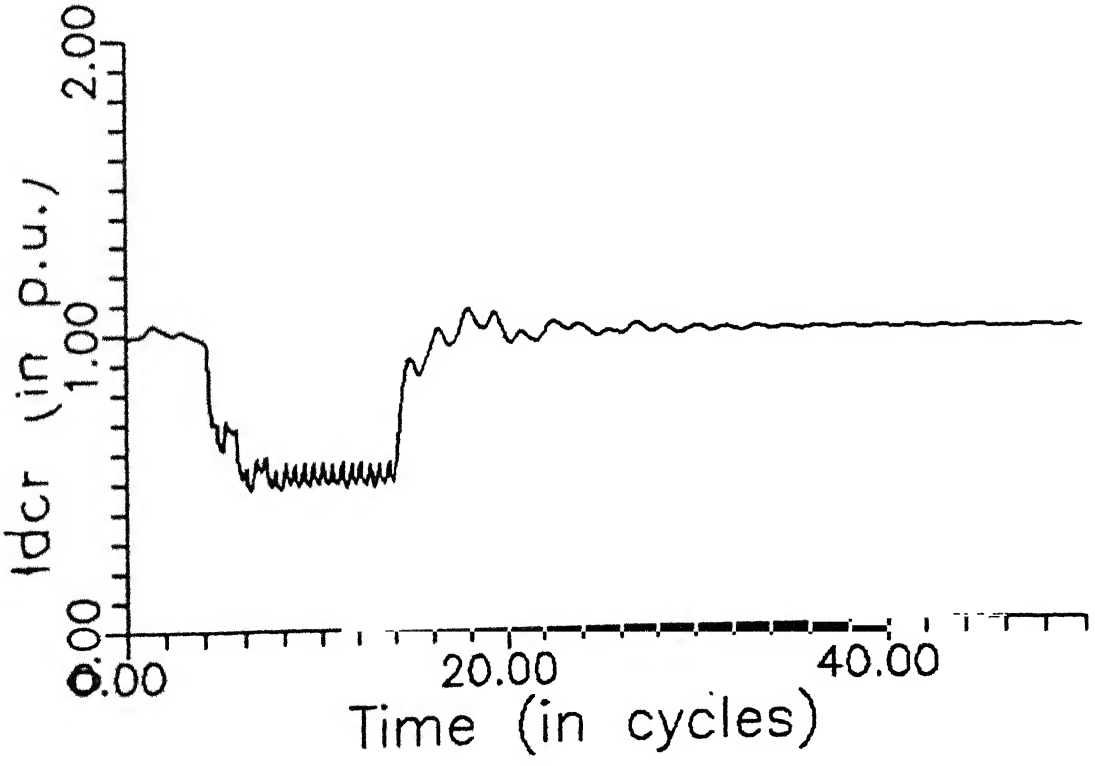


FIG. 4.32 RECTIFIER TERMINAL DC CURRENT FOR CASE 3

(4.32). Similarly, the inverter dc voltage and current are shown in Figures (4.33) & (4.34). The harmonic components of inverter ac voltage,ac current, dc voltage, dc current are shown in Figures (4.35) to (4.38) respectively.

(4) 50% dip in all phases at rectifier

The Figures (4.39) to (4.42) show the rectifier dc voltage & dc current , inverter dc voltage & dc current respectively. The harmonic analysis of inverter ac voltage, ac current, dc voltage, dc current are given in Figures (4.43) to (4.46).

(5) 99% dip in one phase at inverter end

Figures (4.47) and (4.48) show the rectifier average dc voltage and dc current. The invreter average dc voltage and dc current are shown in Figures (4.49) and (4.50). The harmonic spectrum of inverter ac voltage, ac current, dc volatge, dc current are given in Figures (4.51) to (4.54). Due to the fault 2nd and 3rd harmonic components are generated in the dc current and 2nd harmonic in dc voltage.

(6) 99% dip in two phases at invereter

The waveforms of average dc voltage, dc current at rectifier terminal and average dc voltage, dc current at inverter terminal are shown in Figures (4.55) to (4.58) respectively. The harmonic spectrum of inverter ac volatge, ac current, dc voltage, dc current are given in Figures (4.59) to (4.62). During fault the 2nd and 3rd harmonics are generated in the inverter ac voltage and

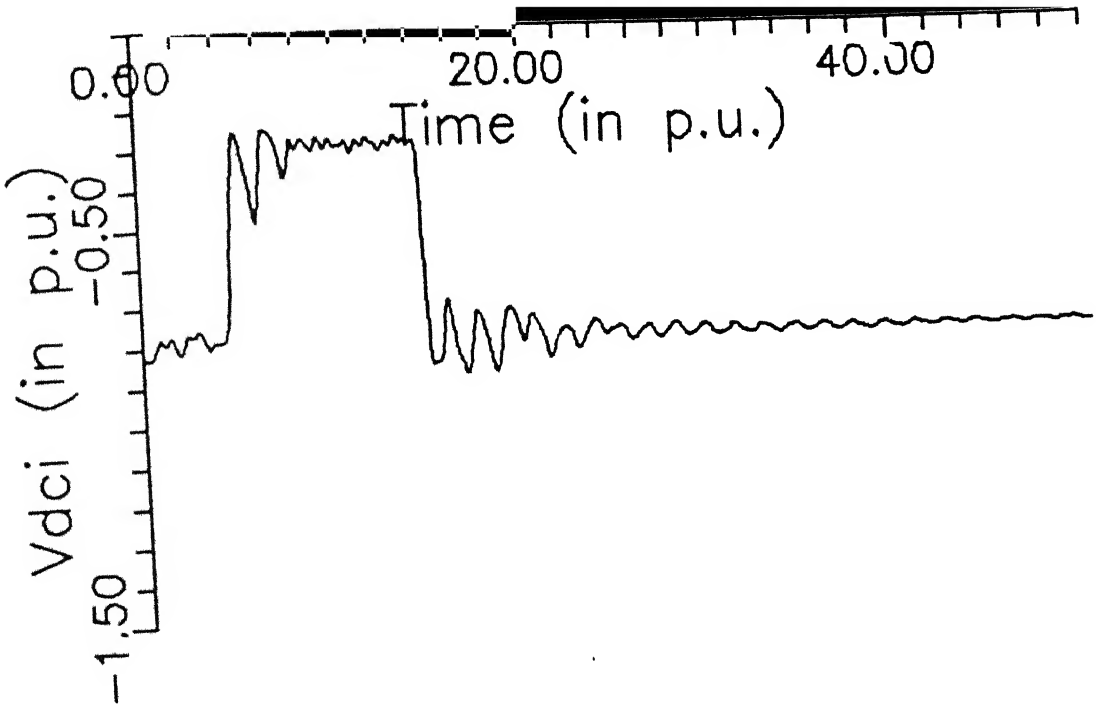


FIG. 4.33 INVERTER TERMINAL DC VOLTAGE FOR CASE 3

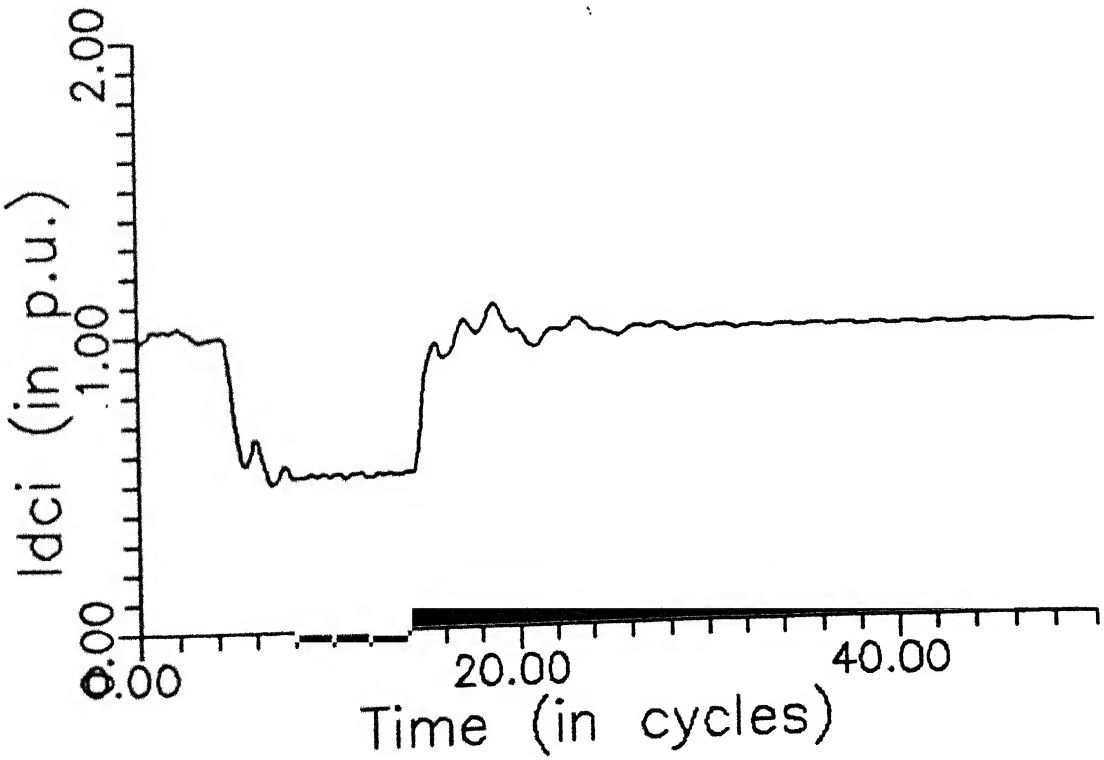


FIG. 4.34 INVERTER TERMINAL DC CURRENT FOR CASE 3

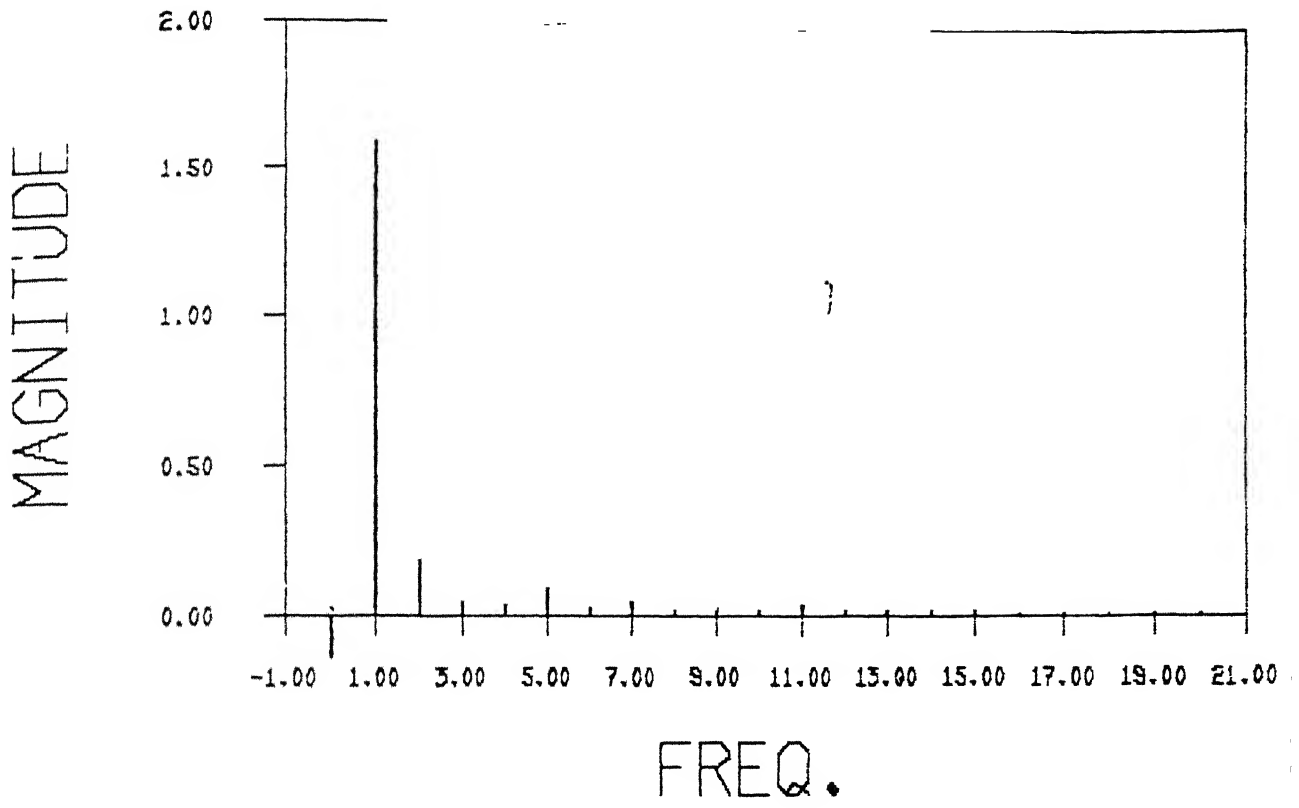


FIG. 4.35 HARMONIC COMPONENTS OF INVERTER AC VOLTAGE FOR CASE 3

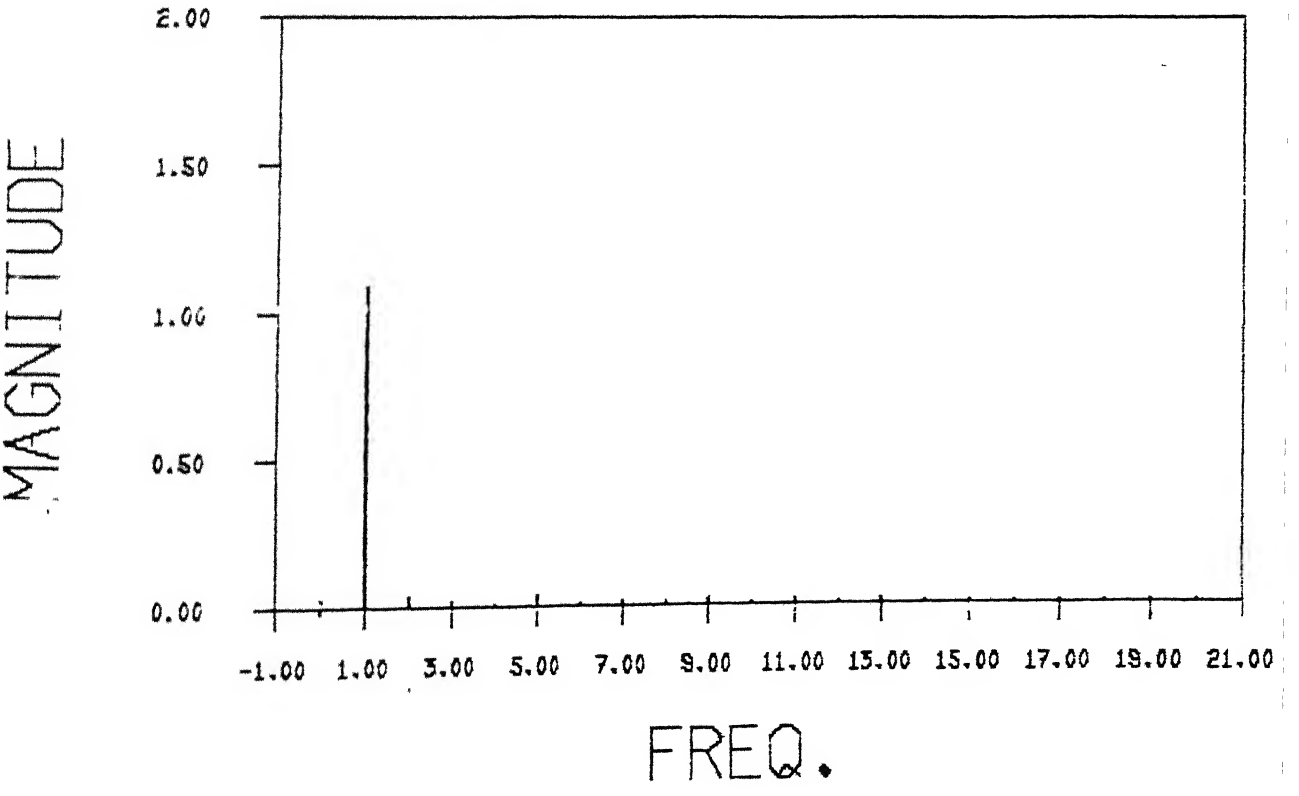


FIG. 4.36 HARMONIC COMPONENTS OF INVERTER AC CURRENT FOR CASE

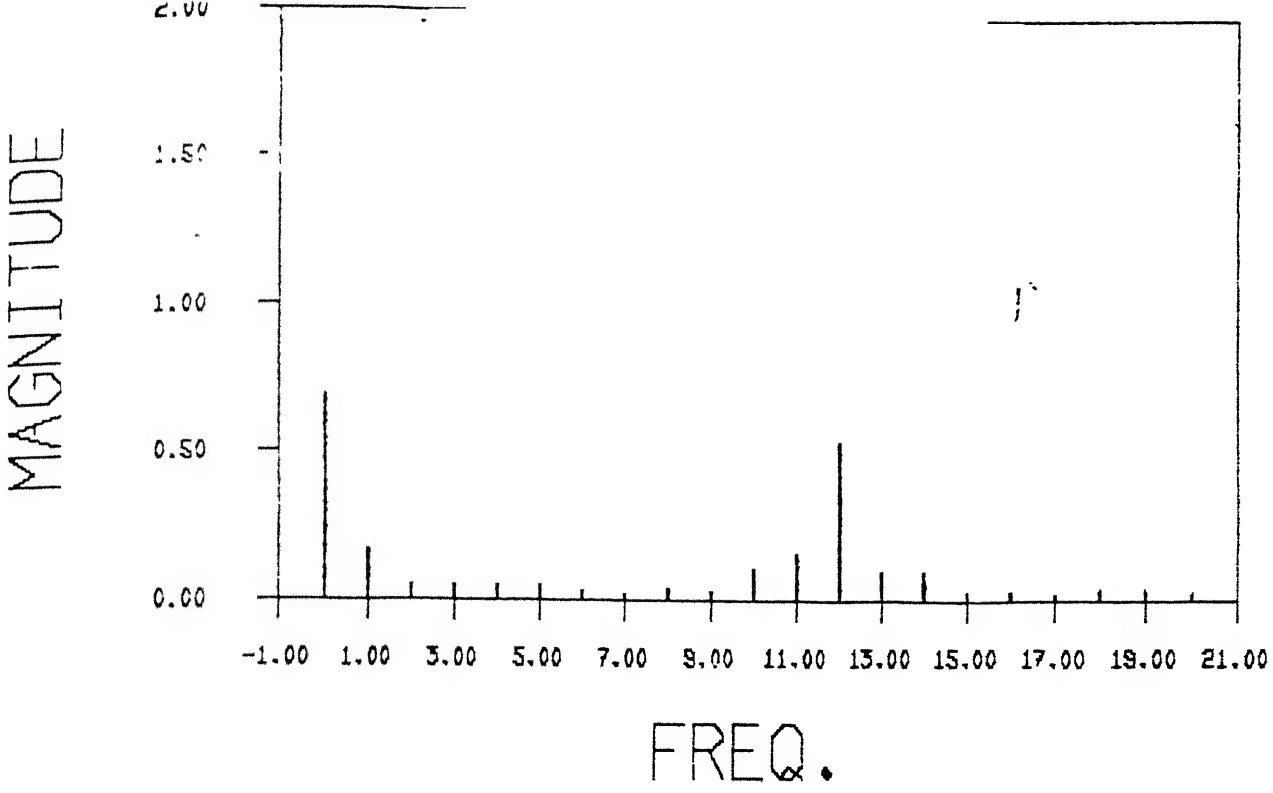


FIG. 4.37 HARMONIC COMPONENTS OF INVERTER DC VOLTAGE FOR CASE 3

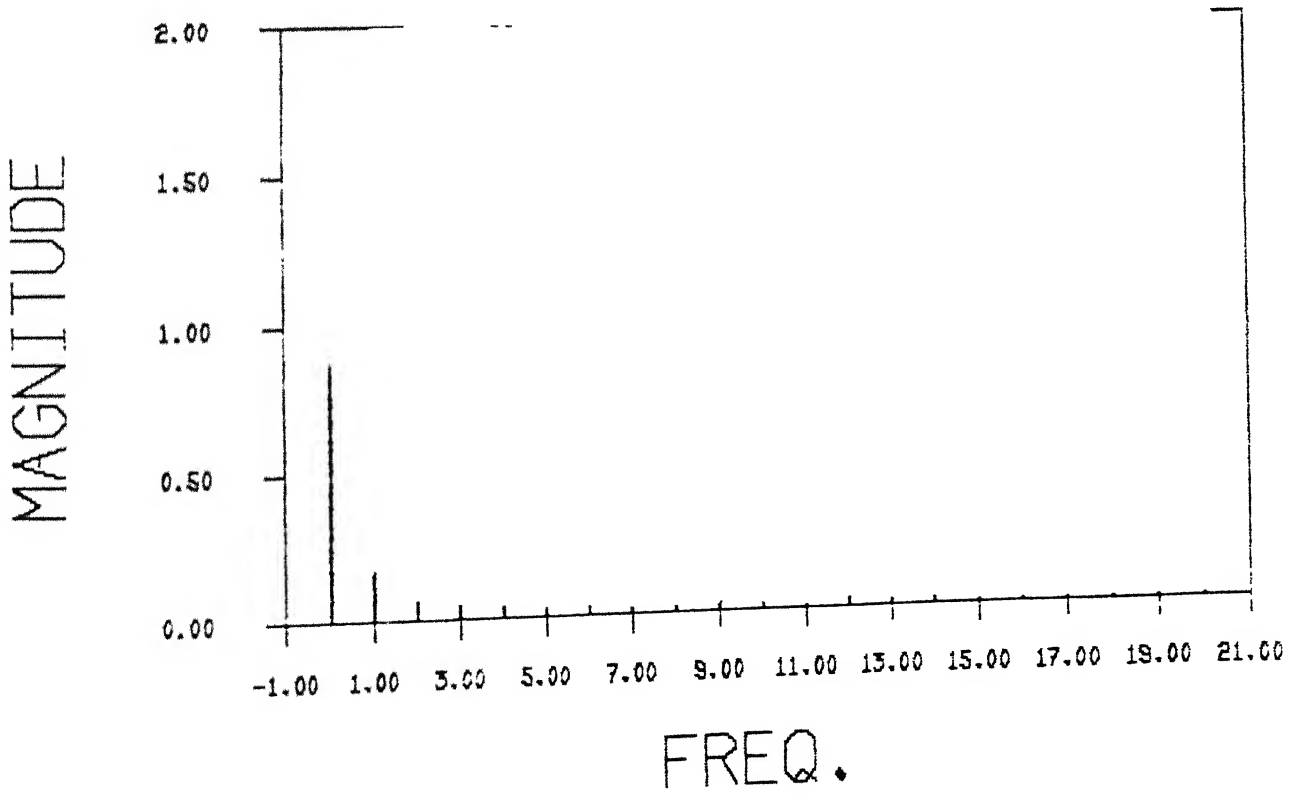


FIG. 4.38 HARMONIC COMPONENTS OF INVERTER DC CURRENT FOR CASE 3

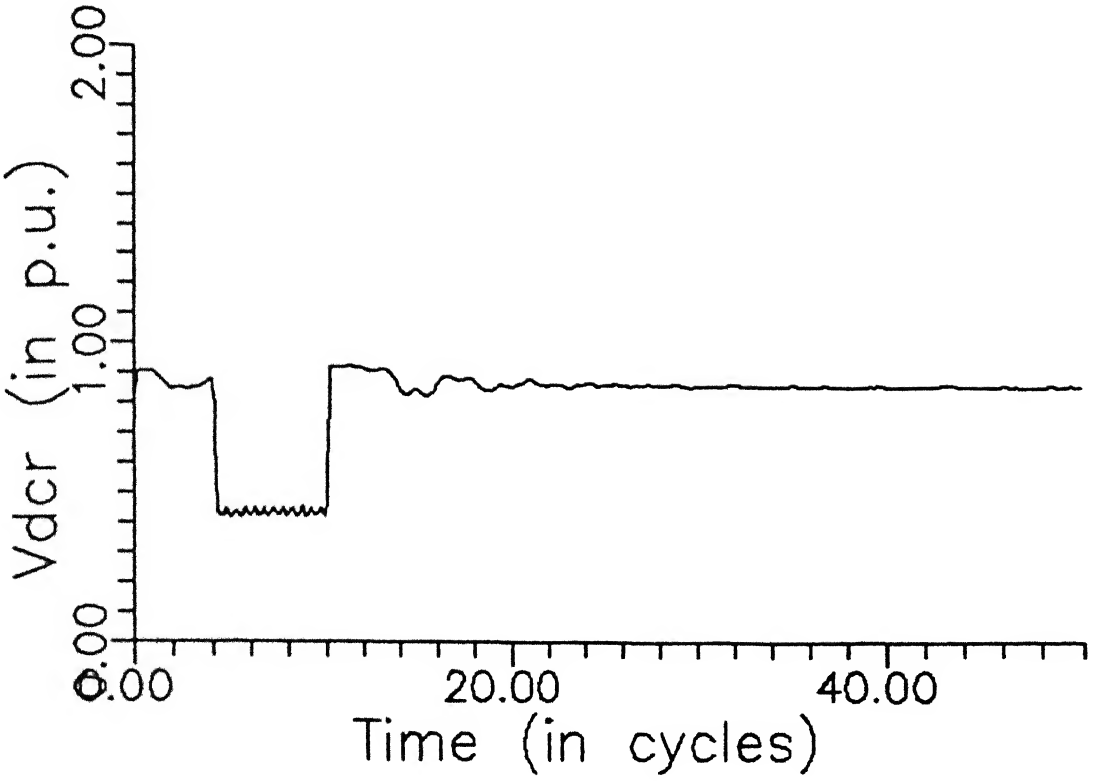


FIG. 4.39 RECTIFIER TERMINAL DC VOLTAGE FOR CASE 4

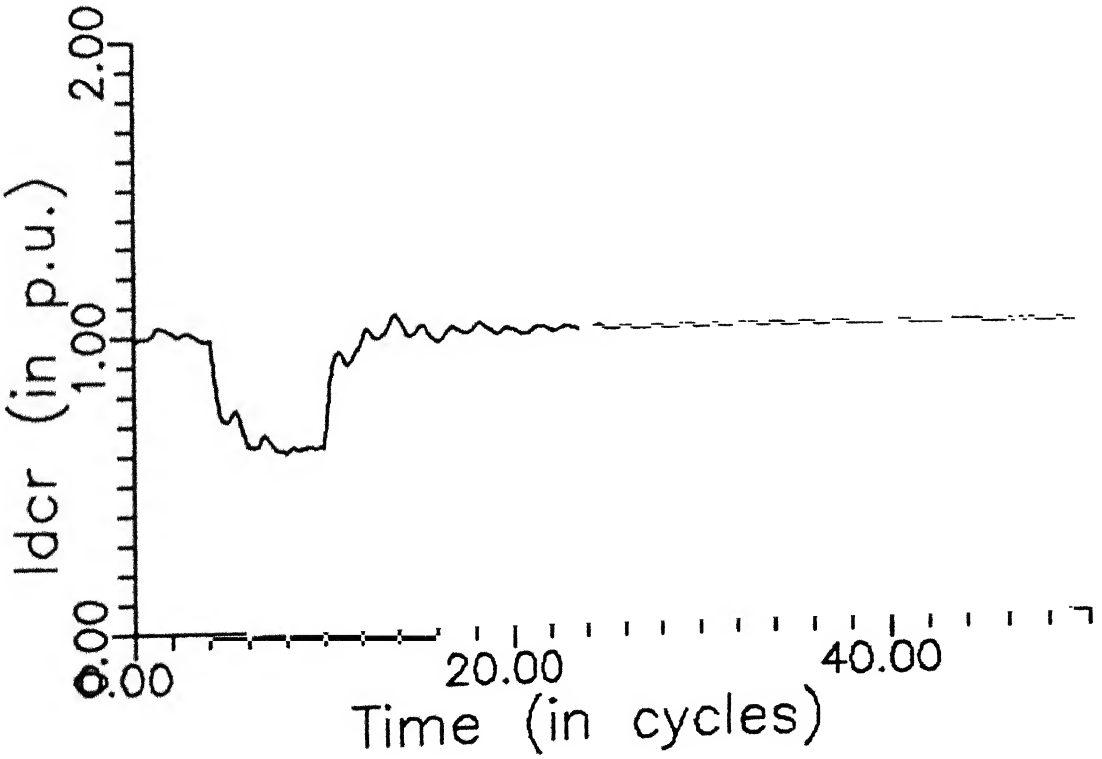


FIG. 4.40 RECTIFIER TERMINAL DC CURRENT FOR CASE 4

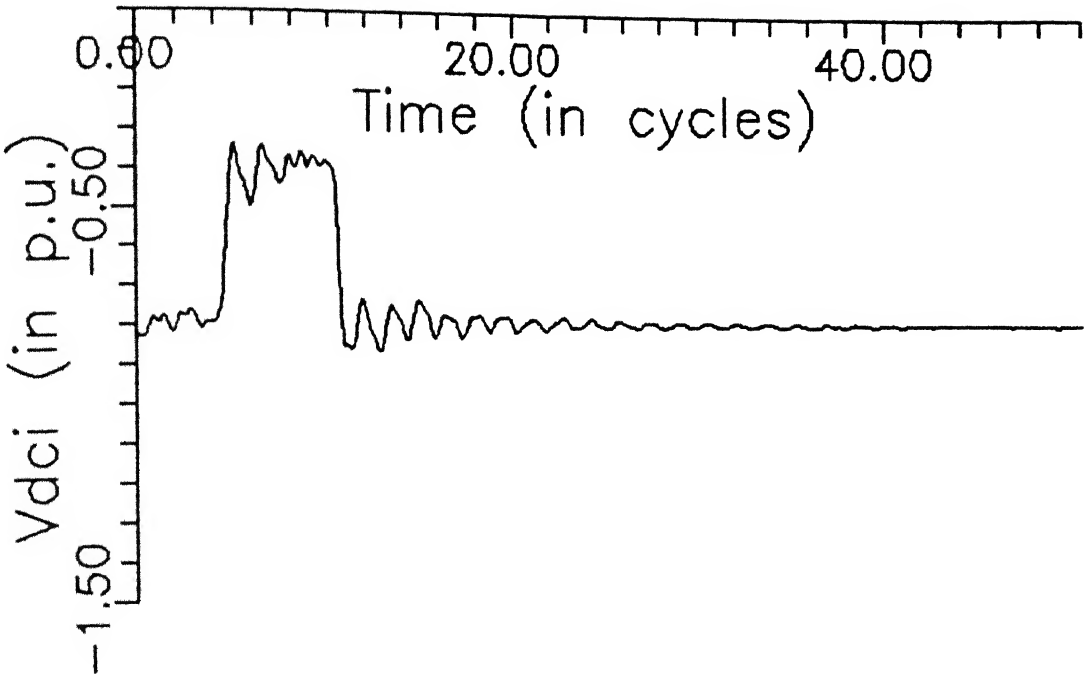


FIG. 4.41 INVERTER TERMINAL DC VOLTAGE FOR CASE 4

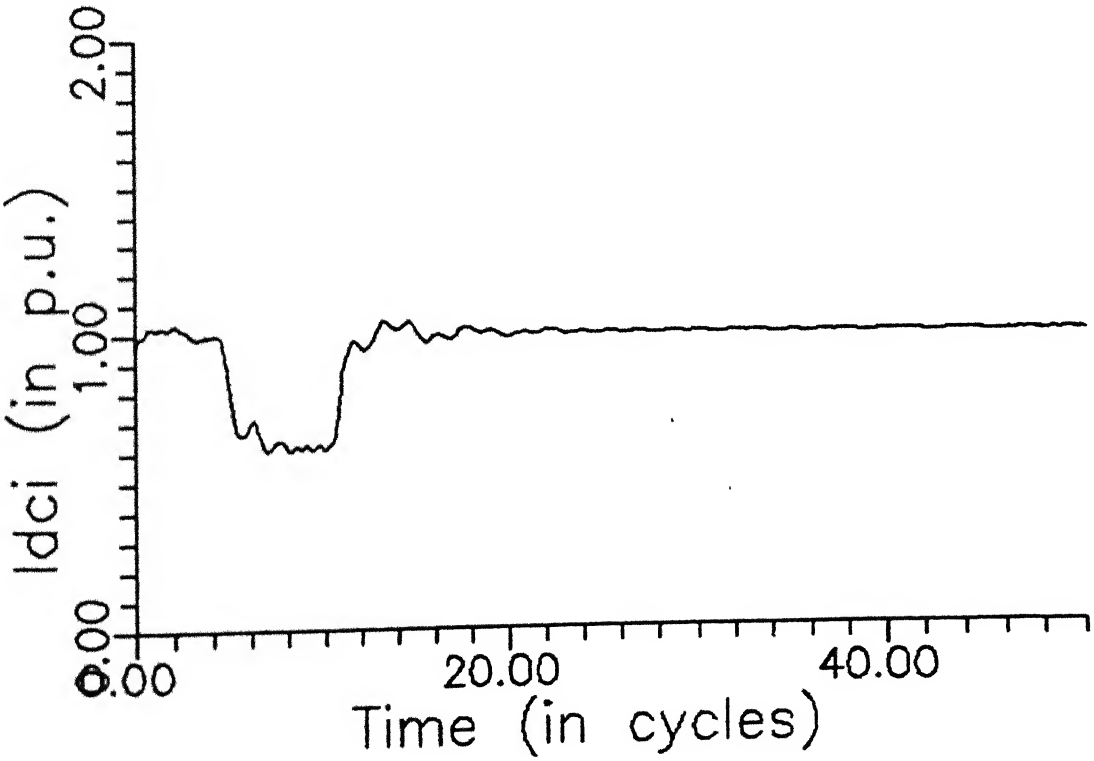


FIG. 4.42 INVERTER TERMINAL DC CURRENT FOR CASE 4

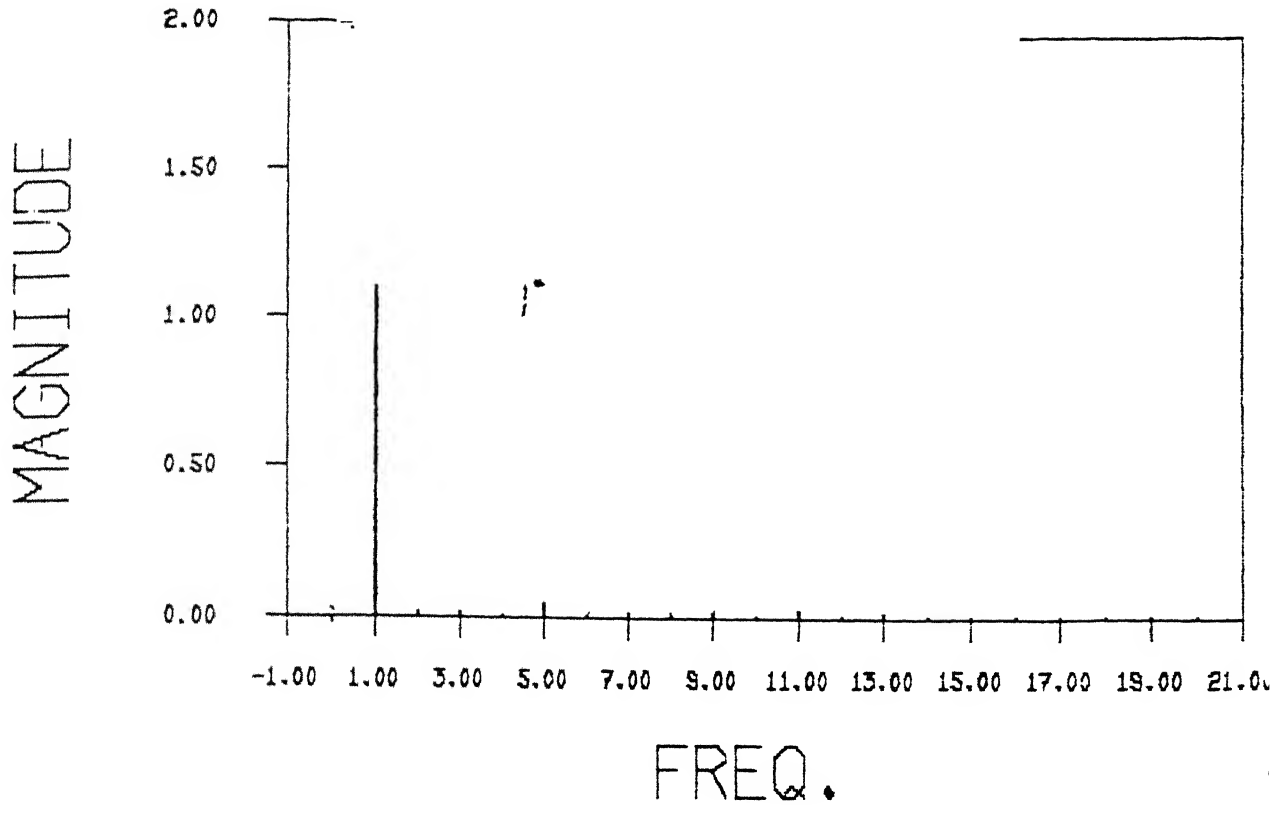


FIG. 4.43 HARMONIC COMPONENTS OF INVERTER AC VOLTAGE FOR CASE 4

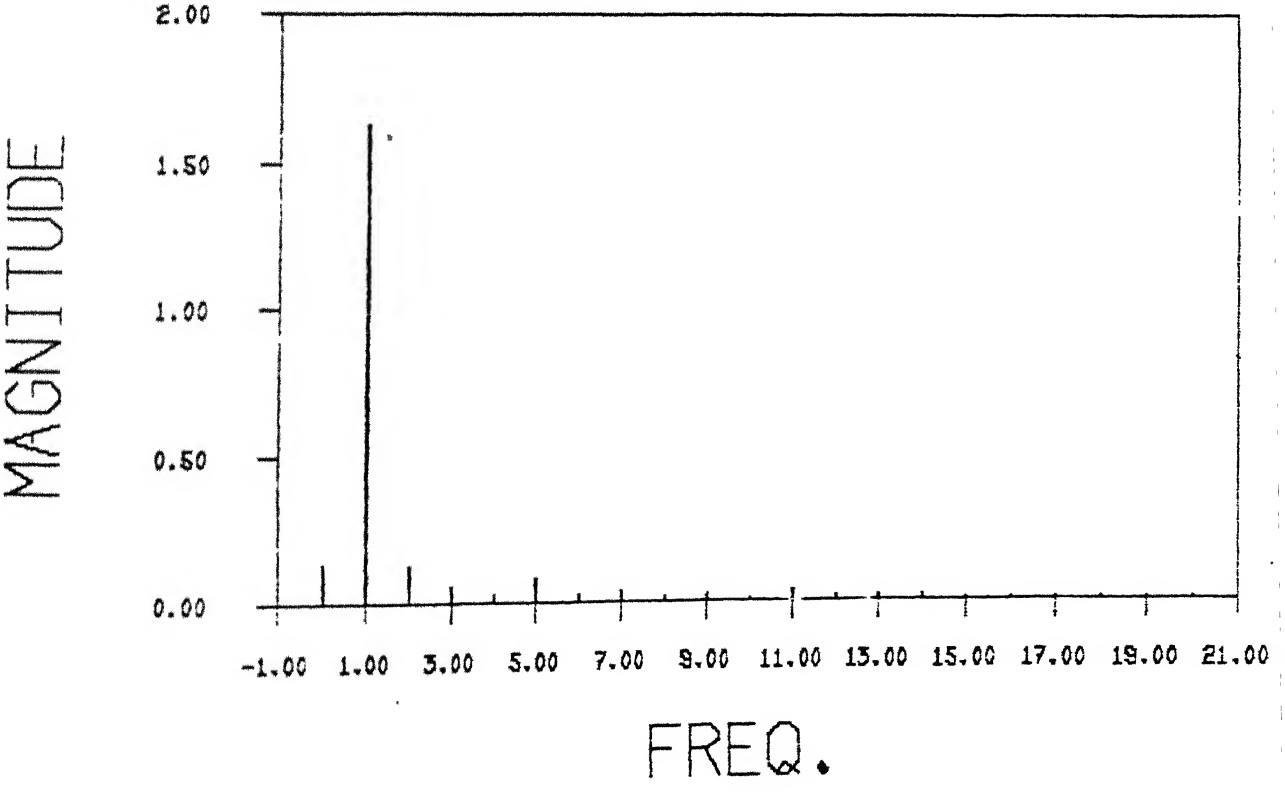


FIG. 4.44 HARMONIC COMPONENTS OF INVERTER AC CURRENT FOR CASE

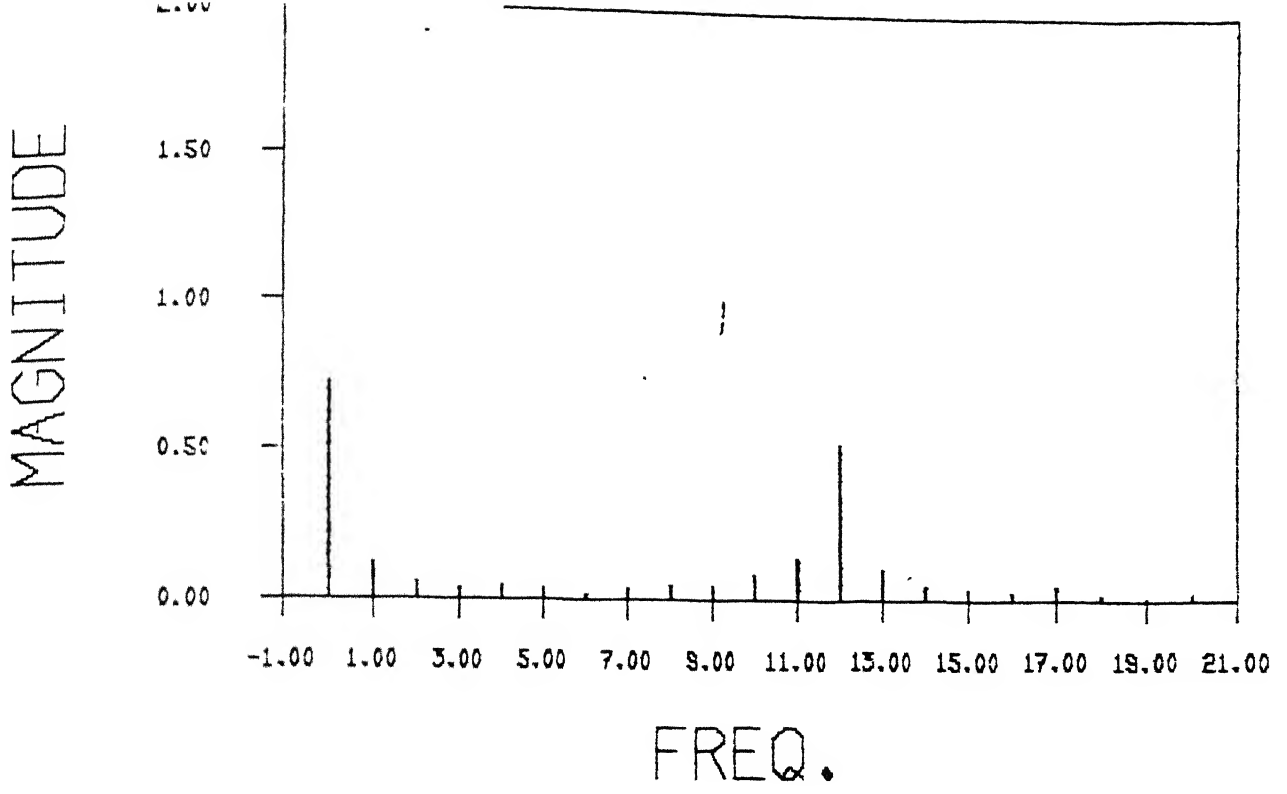


FIG. 4.45 HARMONIC COMPONENTS OF INVERTER DC VOLTAGE FOR CASE 4

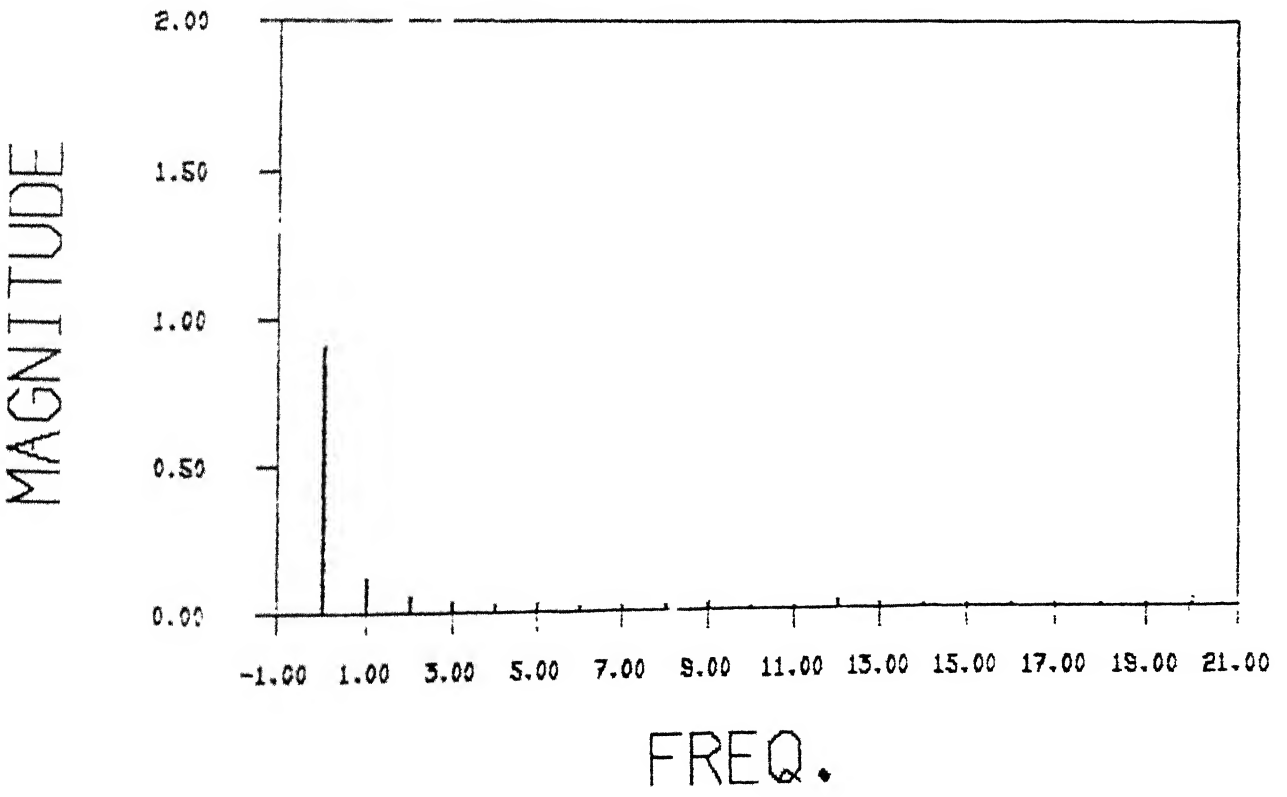


FIG. 4.46 HARMONIC COMPONENTS OF INVERTER DC CURRENT FOR CASE 4

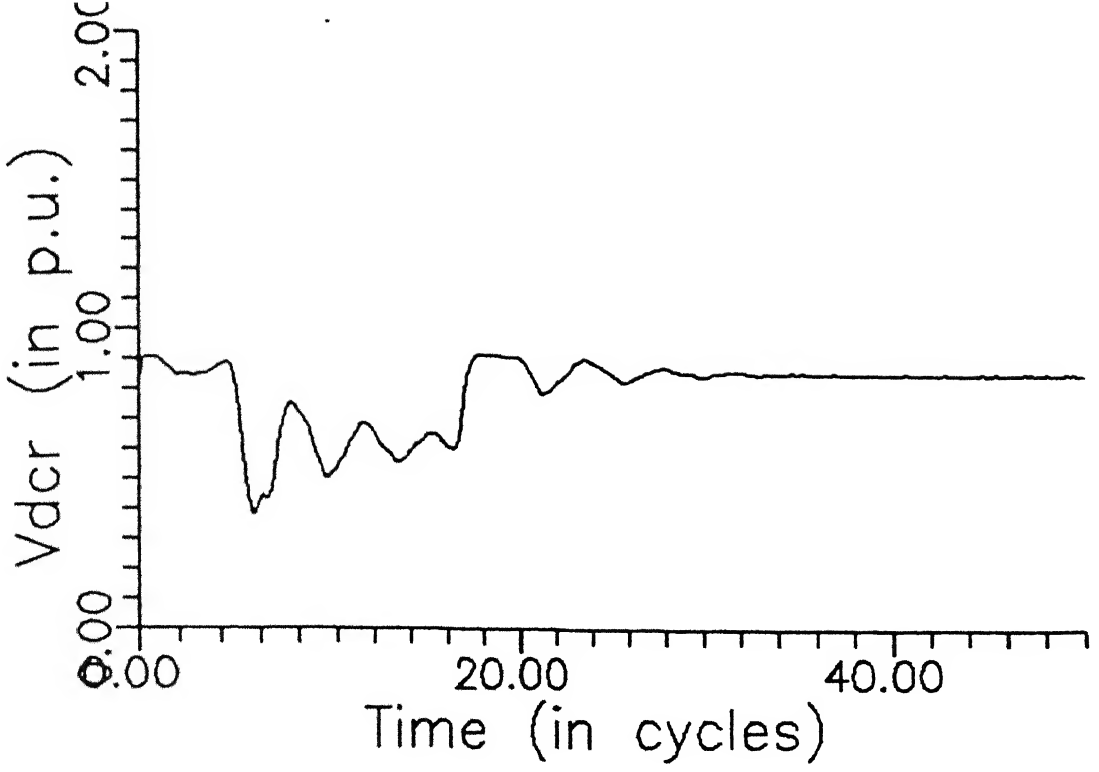


FIG. 4.47 RECTIFIER TERMINAL DC VOLTAGE FOR CASE 5

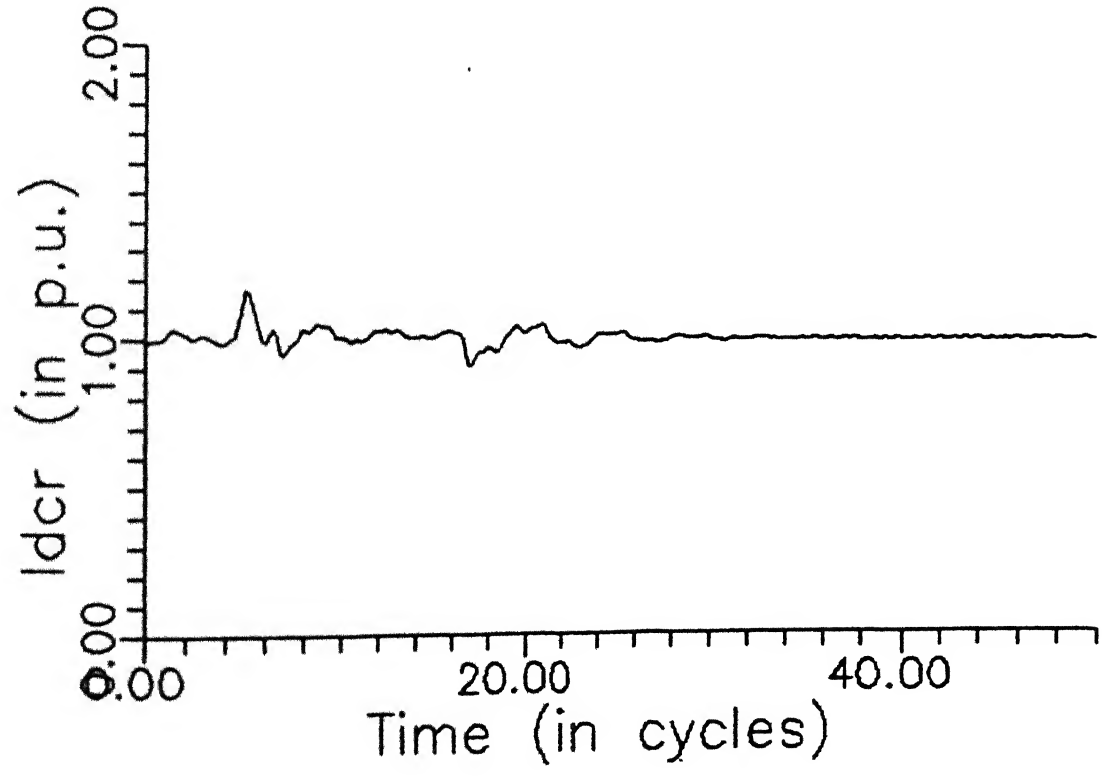


FIG. 4.48 RECTIFIER TERMINAL DC CURRENT FOR CASE 5

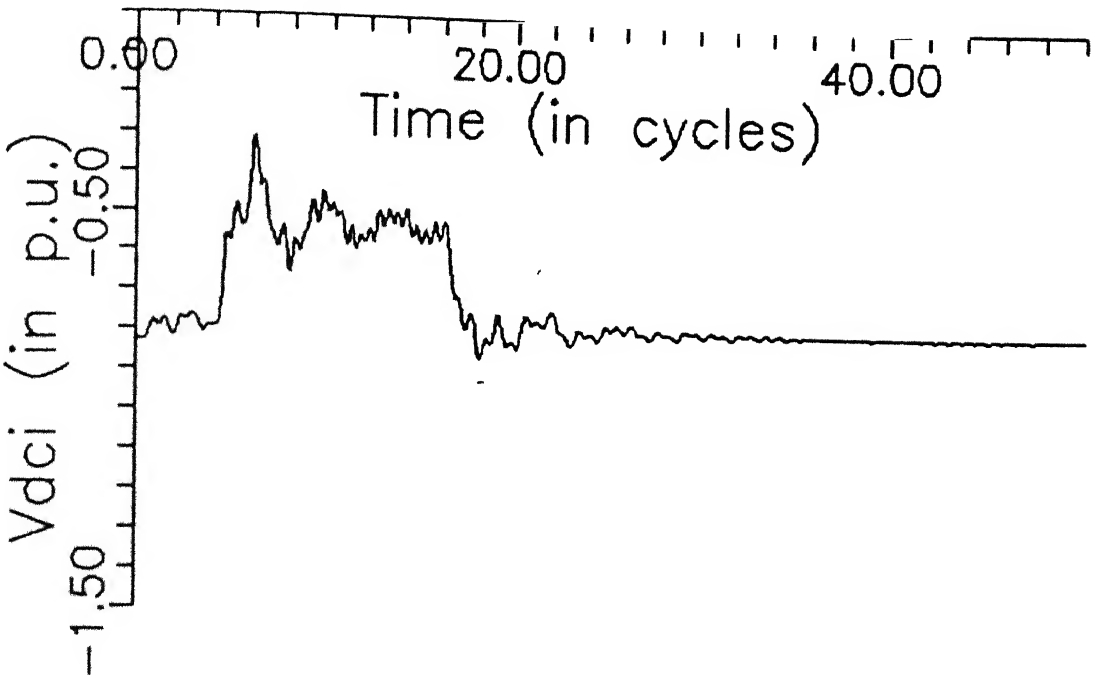


FIG. 4.49 INVERTER TERMINAL DC VOLTAGE FOR CASE 5

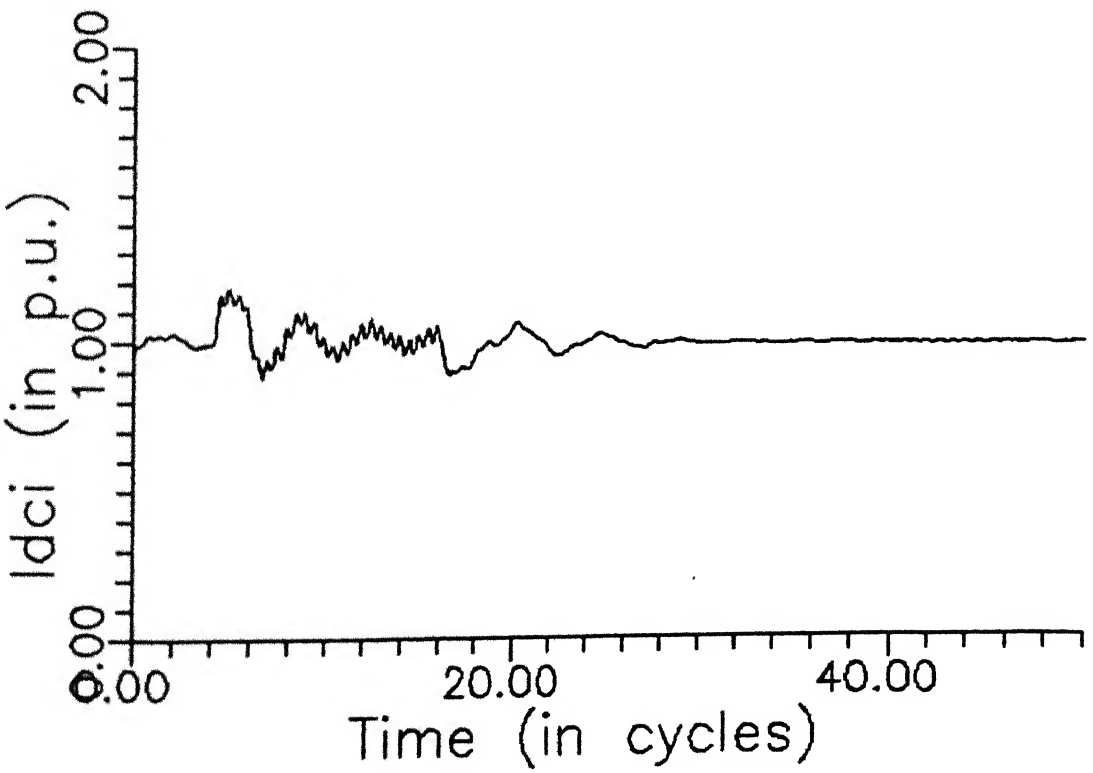


FIG. 4.50 INVERTER TERMINAL DC CURRENT FOR CASE 5

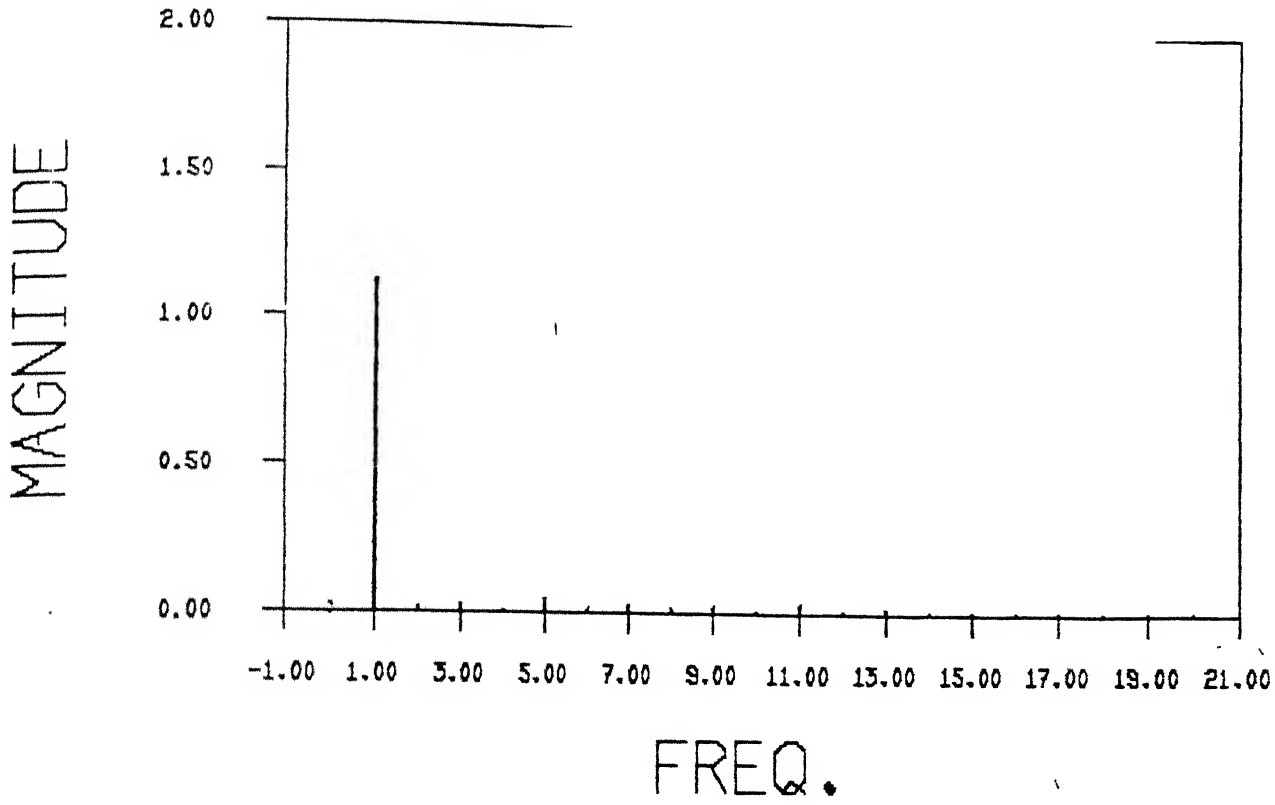


FIG. 4.51 HARMONIC COMPONENTS OF INVERTER AC VOLTAGE FOR CASE 5

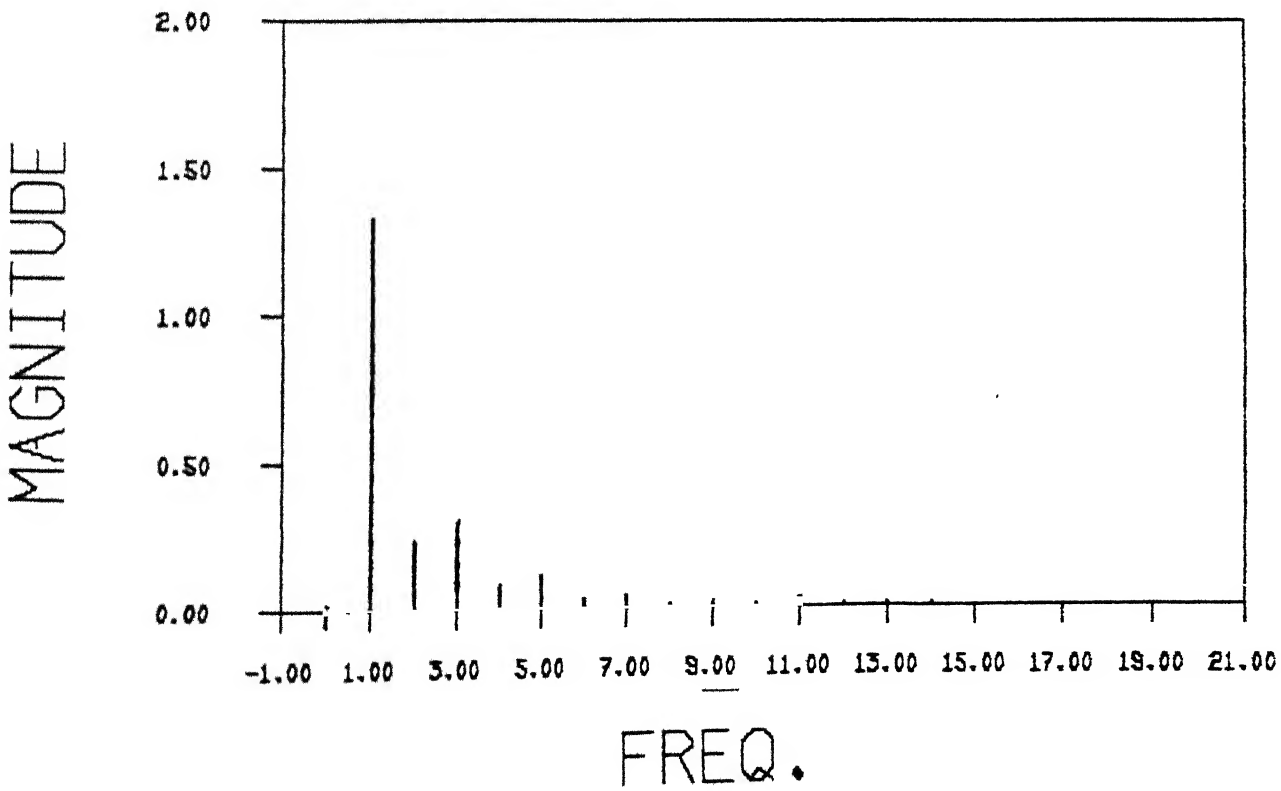


FIG. 4.52 HARMONIC COMPONENTS OF INVERTER AC CURRENT FOR CASE 5

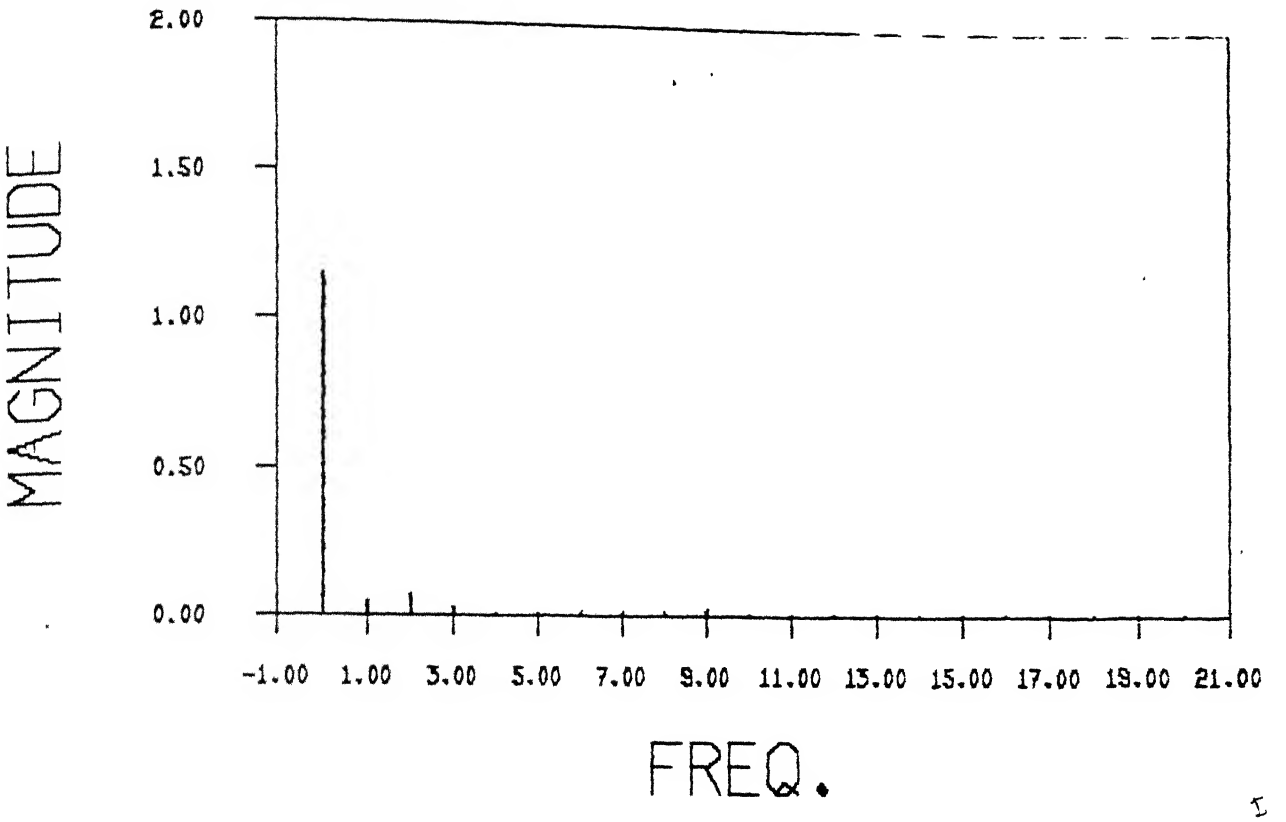


FIG. 4.53 HARMONIC COMPONENTS OF INVERTER DC VOLTAGE FOR CASE 5

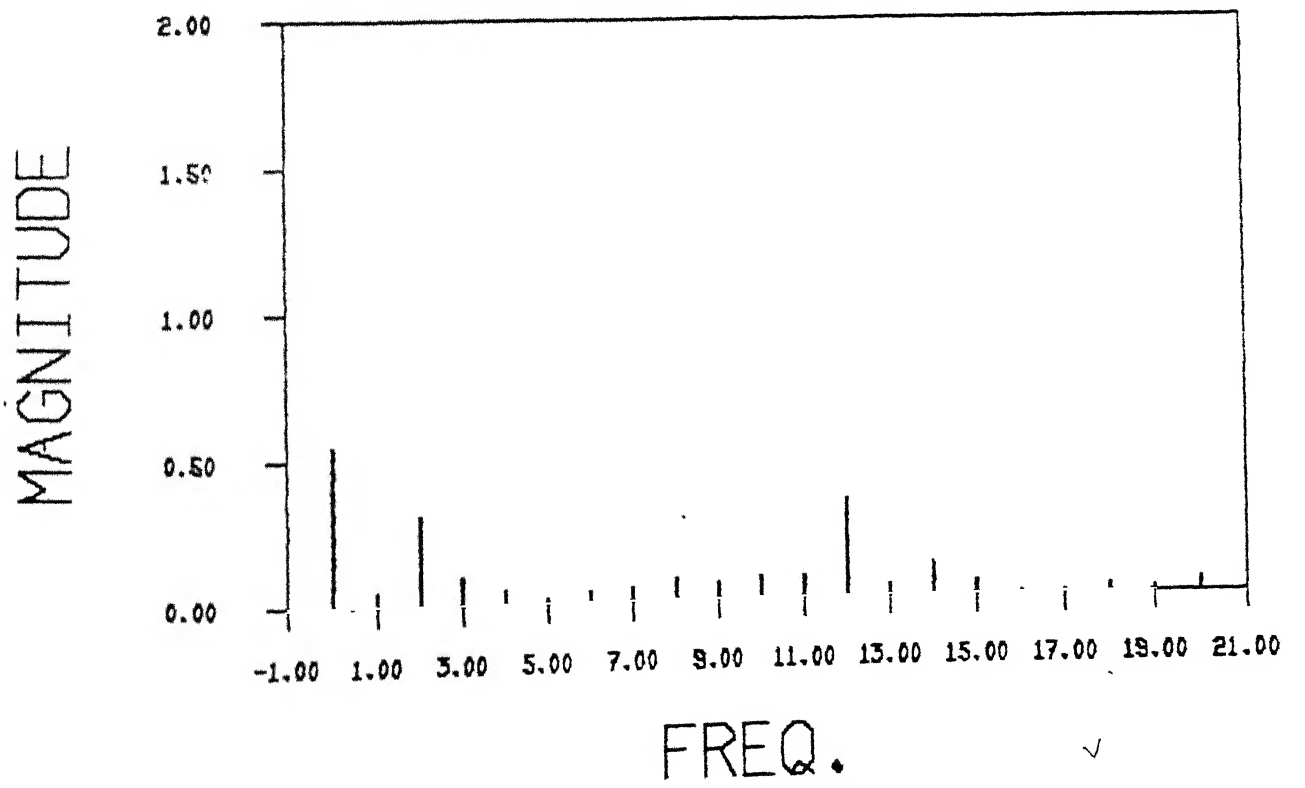


FIG. 4.54 HARMONIC COMPONENTS OF INVERTER DC CURRENT FOR CASE 5

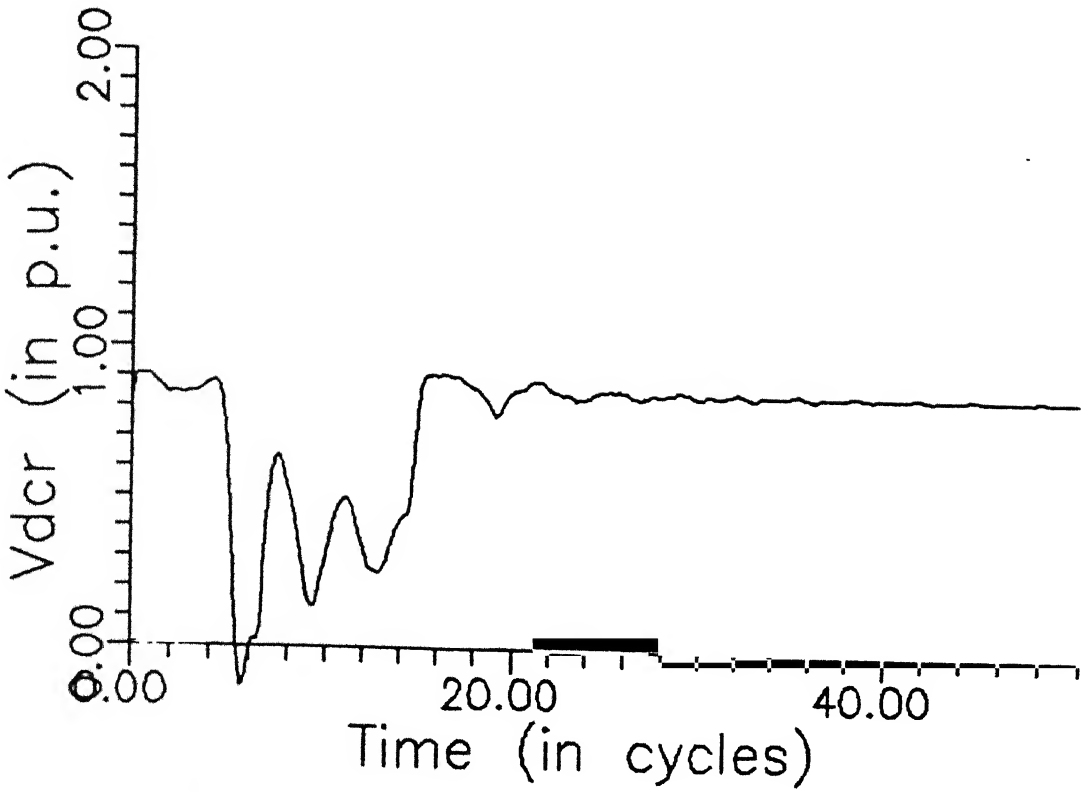


FIG. 4.55 RECTIFIER TERMINAL DC VOLTAGE FOR CASE 6

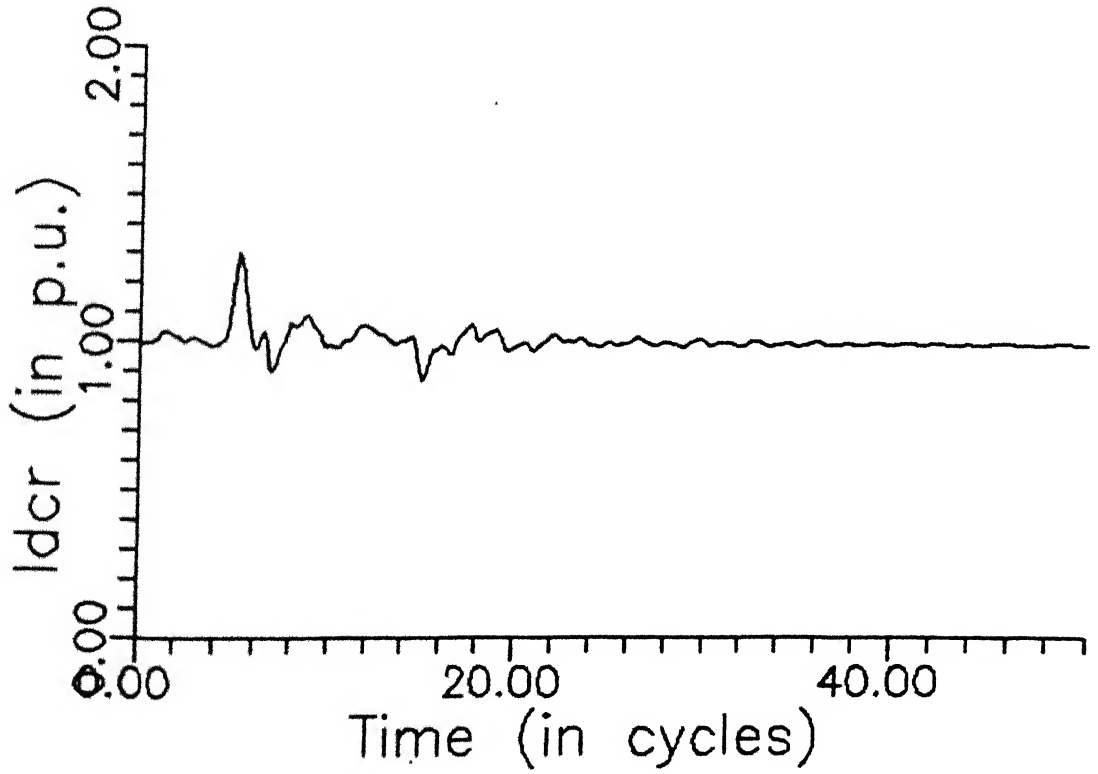


FIG. 4.56 RECTIFIER TERMINAL DC CURRENT FOR CASE 6

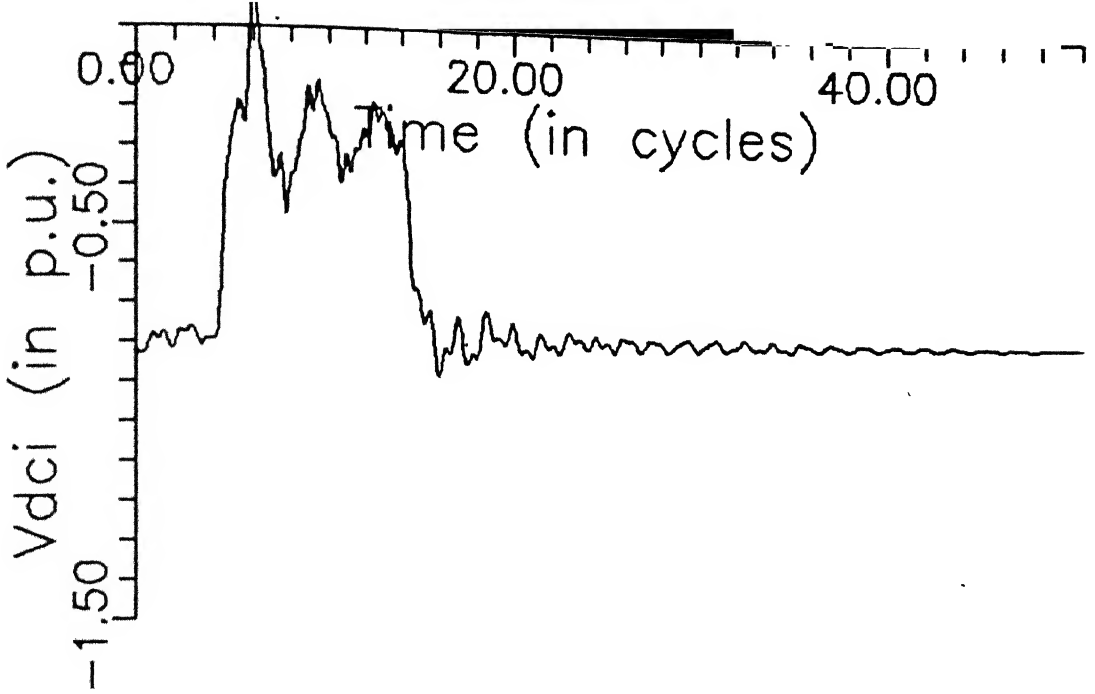


FIG. 4.57 INVERTER TERMINAL DC VOLTAGE FOR CASE 6

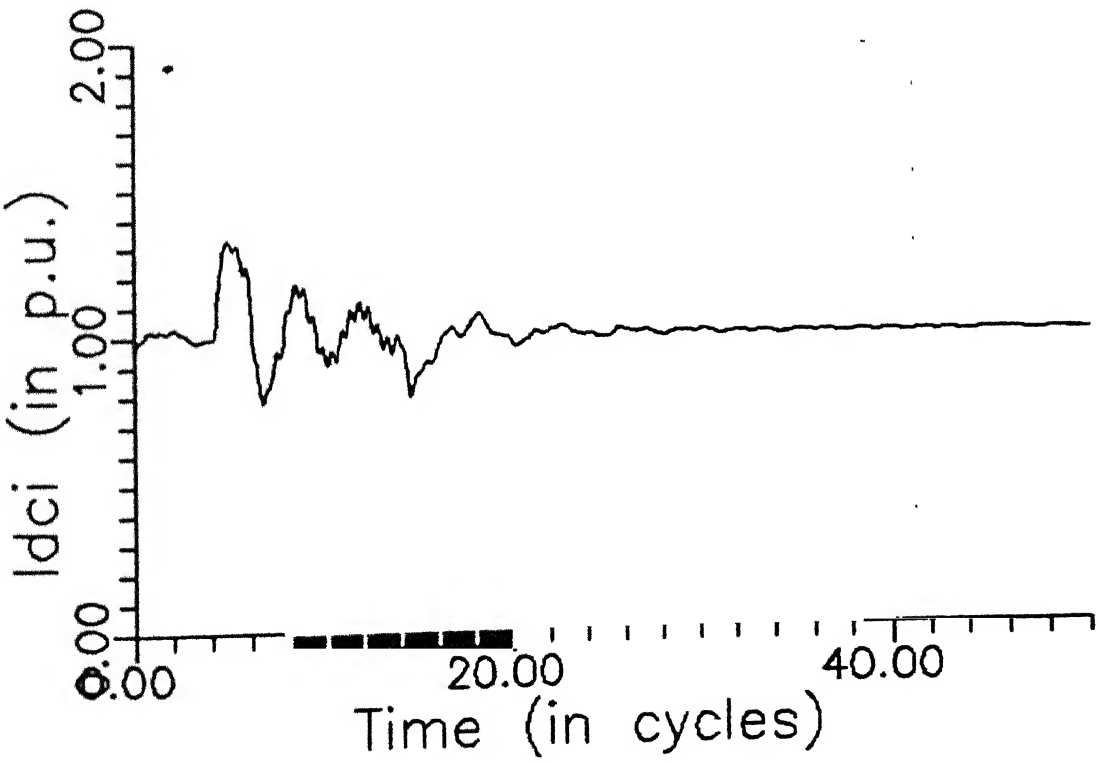


FIG. 4.58 INVERTER TERMINAL DC CURRENT FOR CASE 6

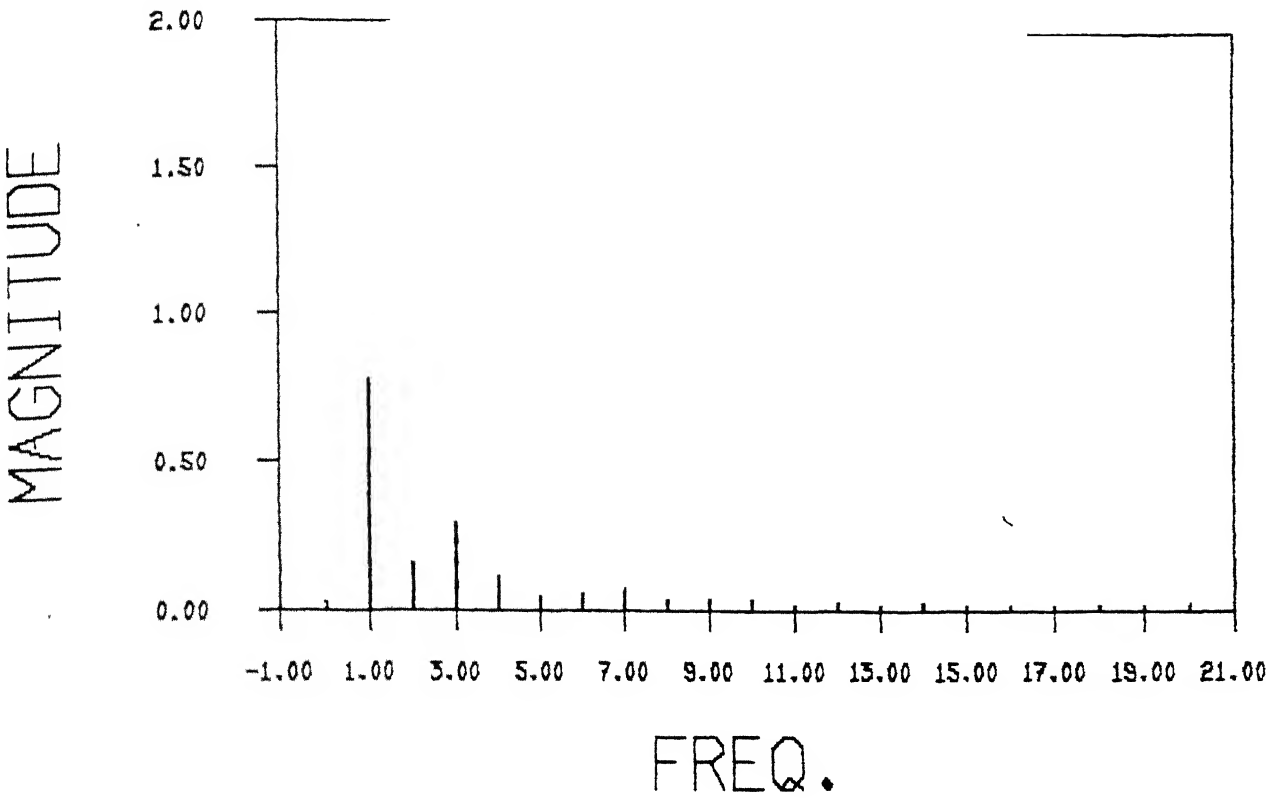


FIG. 4.59 HARMONIC COMPONENTS OF INVERTER AC VOLTAGE FOR CASE 6

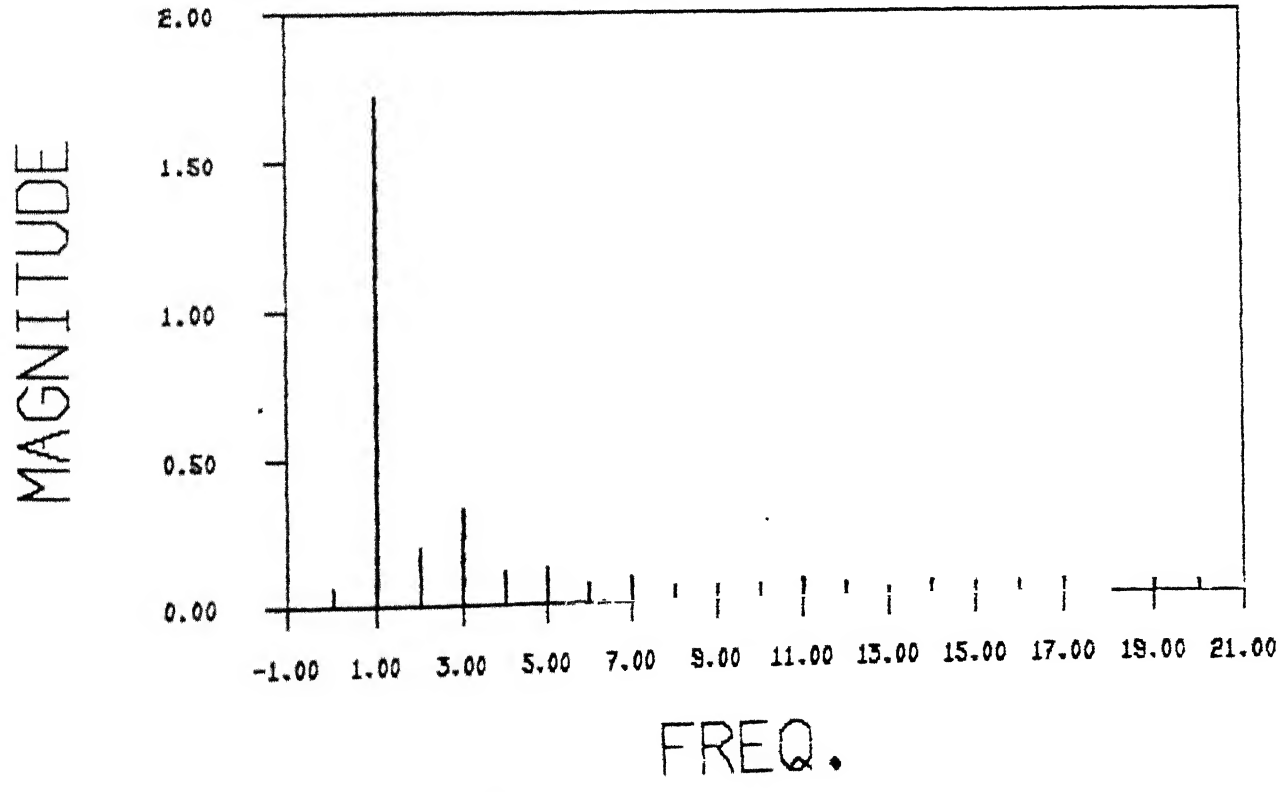


FIG. 4.60 HARMONIC COMPONENTS OF INVERTER AC CURRENT FOR CASE 6

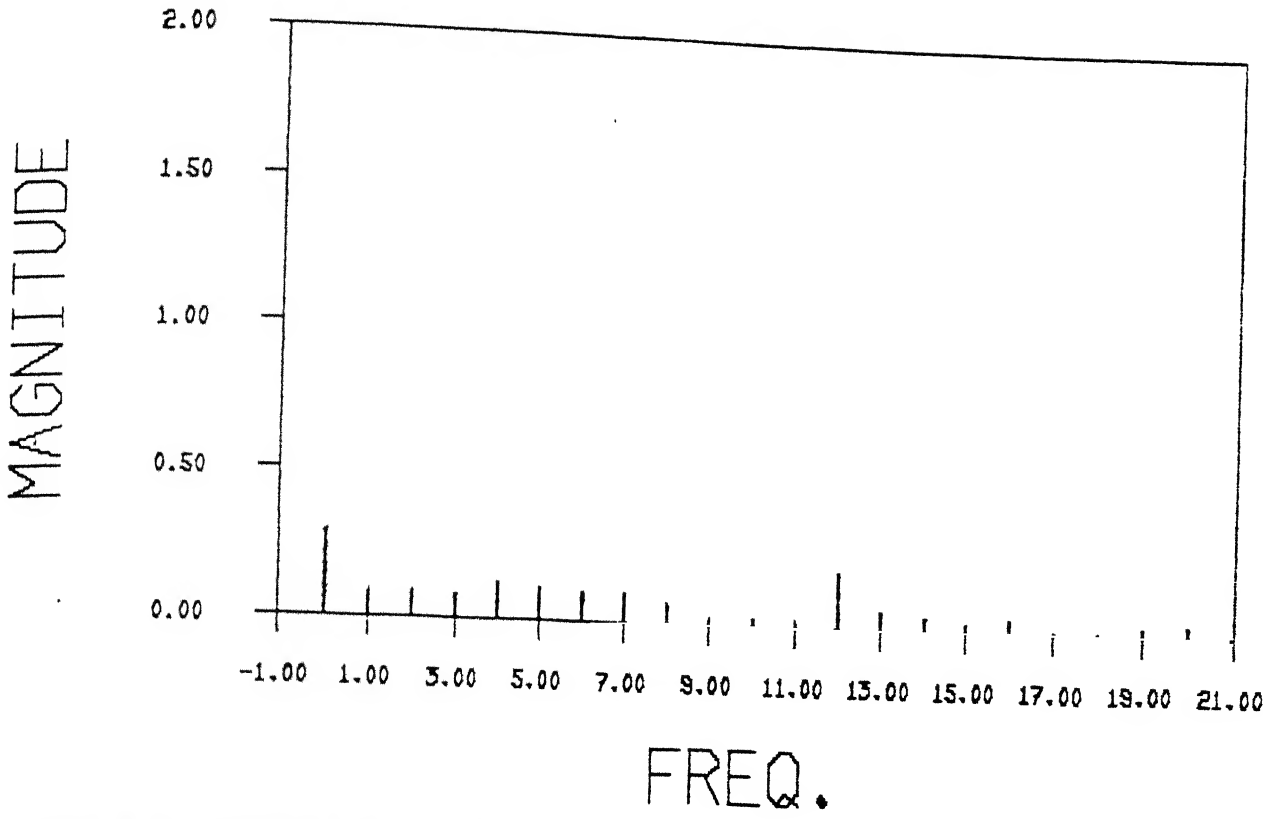


FIG. 4.61 HARMONIC COMPONENTS OF INVERTER DC VOLTAGE FOR CASE 6

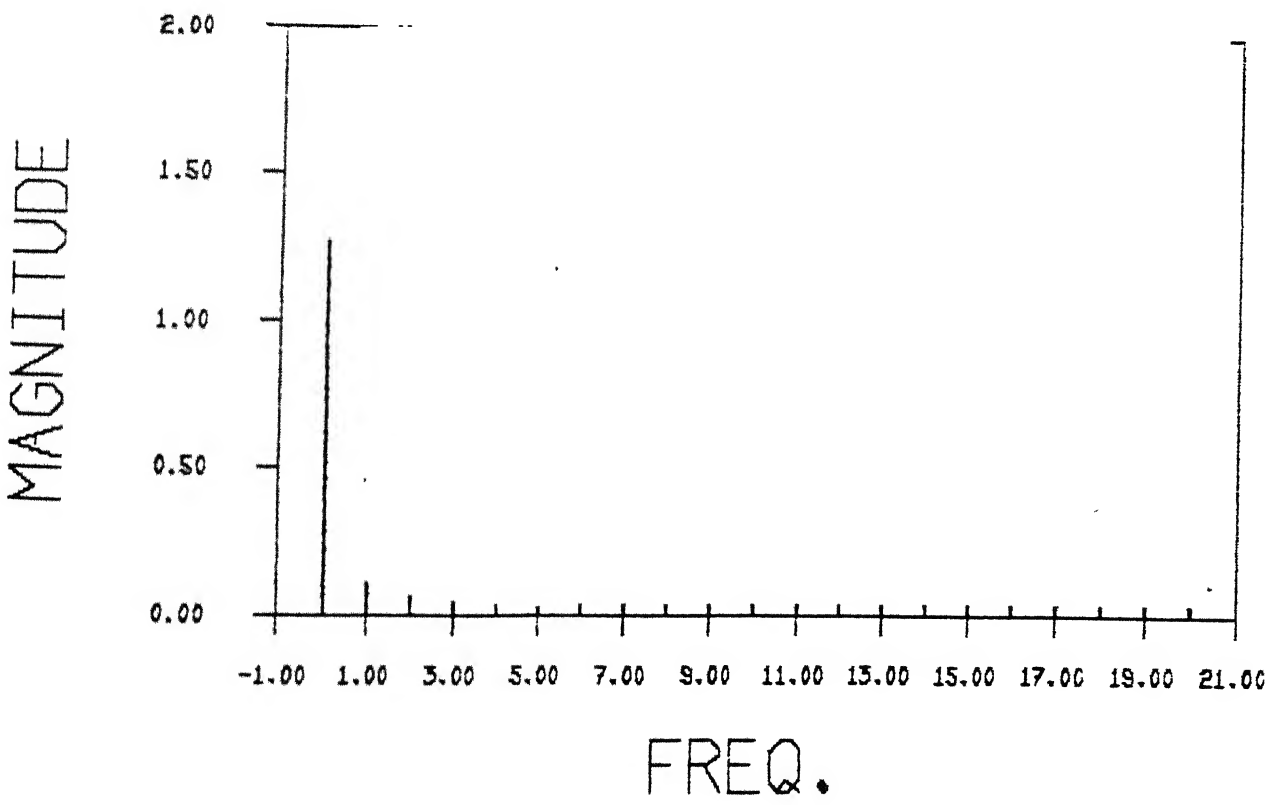


FIG. 4.62 HARMONIC COMPONENTS OF INVERTER DC CURRENT FOR CASE 6

ac current.

(7) 99% dip in all phases at inverter

Figures (4.63) to (4.66) show the rectifier average dc current, dc current and inverter average dc voltage, dc current respectively. The harmonic components of inverter ac voltage, ac current, dc voltage, dc current are shown in Figures (4.67) to (4.70). This fault is very severe but less probable. This is studied for 5 cycle dip only.

(8) 50% dip in all phases at inverter

This fault is known as three phase remote fault. This effect is rather less at inverter than 99% dip at inverter. Figures (4.71) to (4.72) show the rectifier average dc voltage, dc current and inverter average dc voltage, dc current respectively. The harmonic components of inverter ac voltage, ac current, dc voltage, dc current are shown in Figures (4.73a) to (4.74b).

DISCUSSION OF RESULTS

The steady state behaviour of HVDC system with GTO inverter is improved than using GTO converter with an active load. The lower order harmonics are totally eliminated. The dc output voltage have only 11th harmonic component. During disturbances, particularly dips in ac voltage at rectifier end, no extra hormonic components are generated in inverter side quantities. Some harmonics are generated during faults at inverter ac voltage. The power factor is maintained at unity. The comparision of HVDC system with GTO inverter has been made with thyristor inverter.

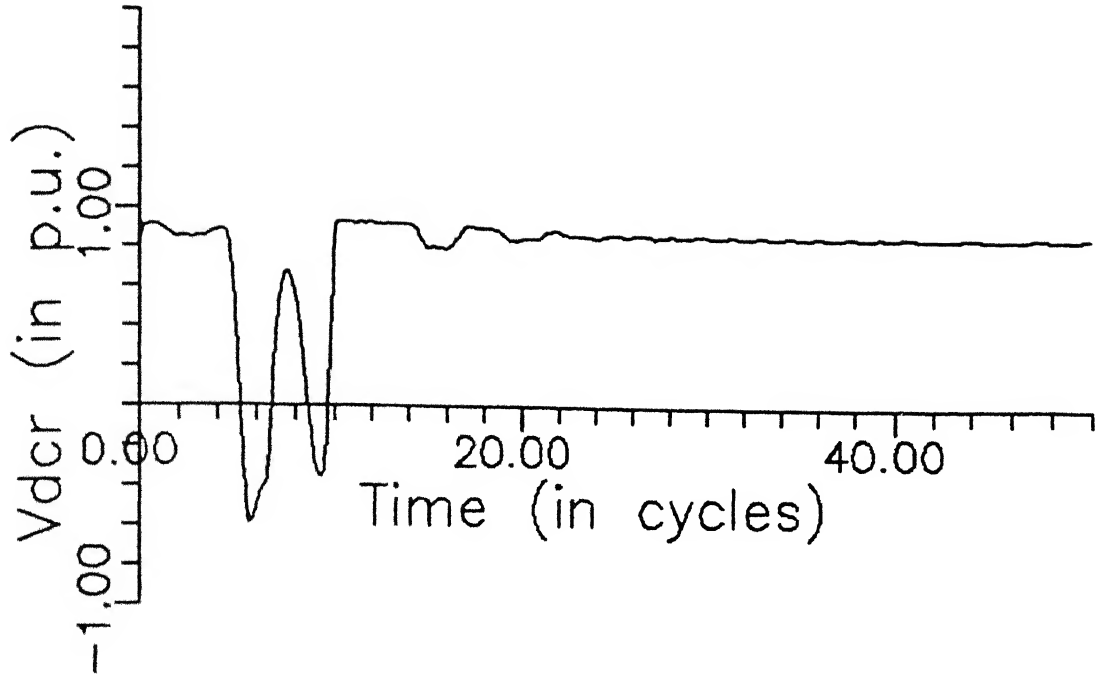


FIG. 4.63 RECTIFIER TERMINAL DC VOLTAGE FOR CASE 7

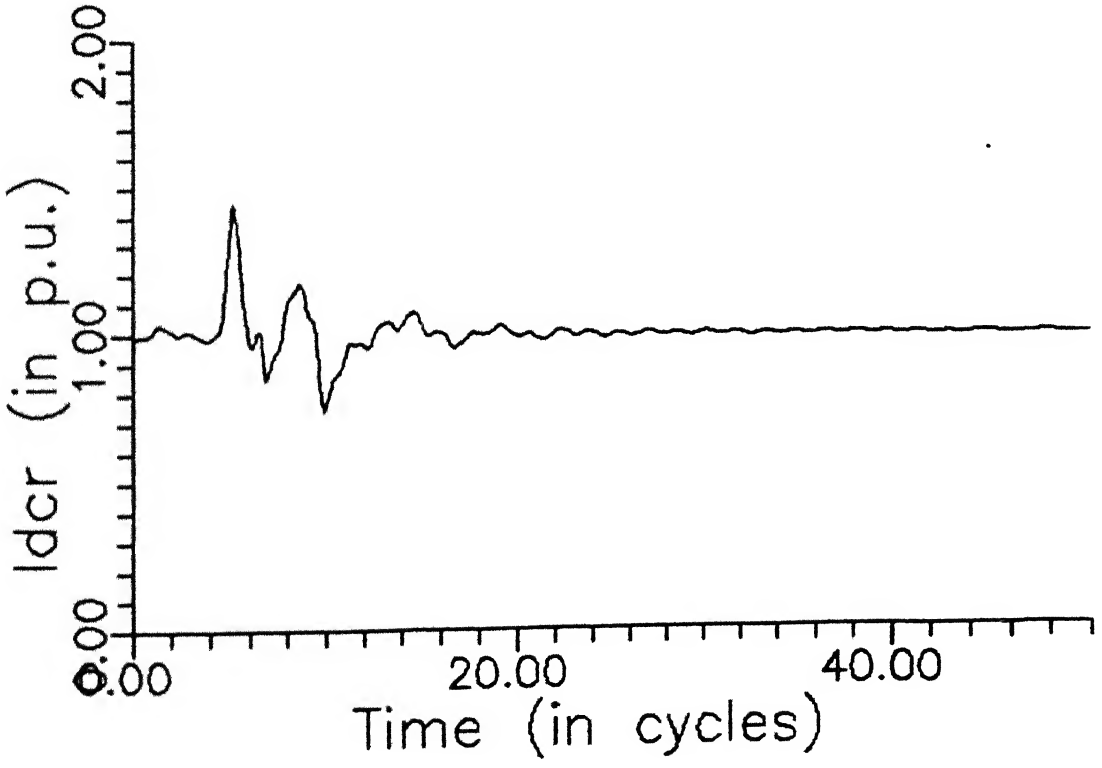


FIG. 4.64 RECTIFIER TERMINAL DC CURRENT FOR CASE 7

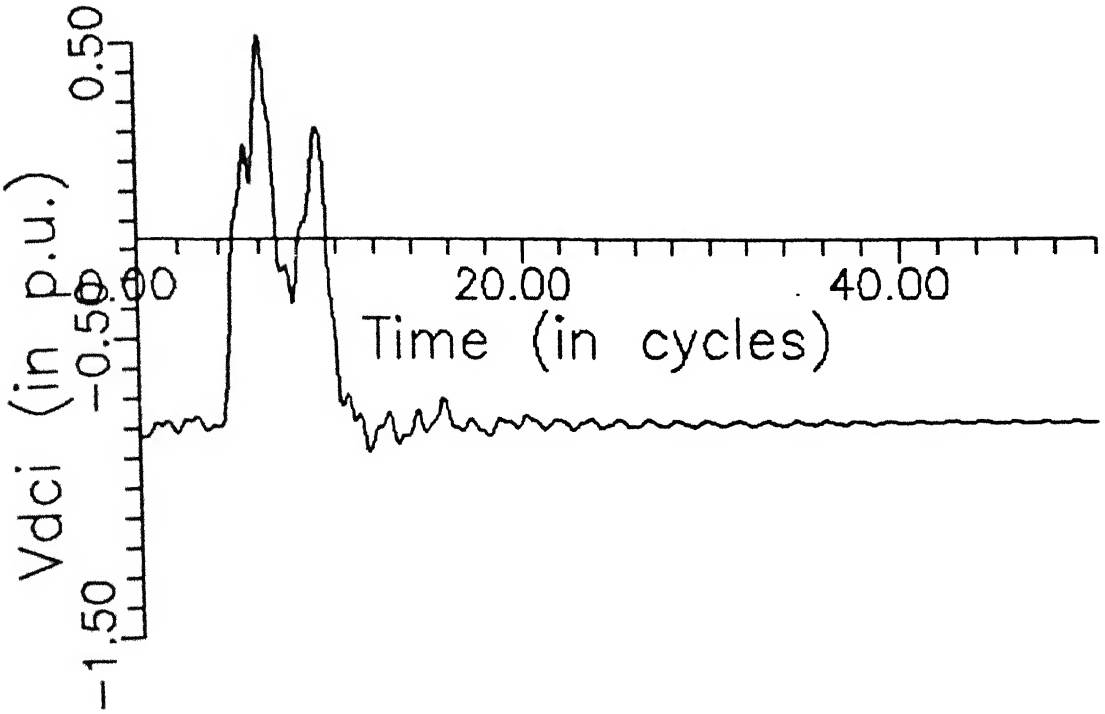


FIG. 4.65 INVERTER TERMINAL DC VOLTAGE FOR CASE 7

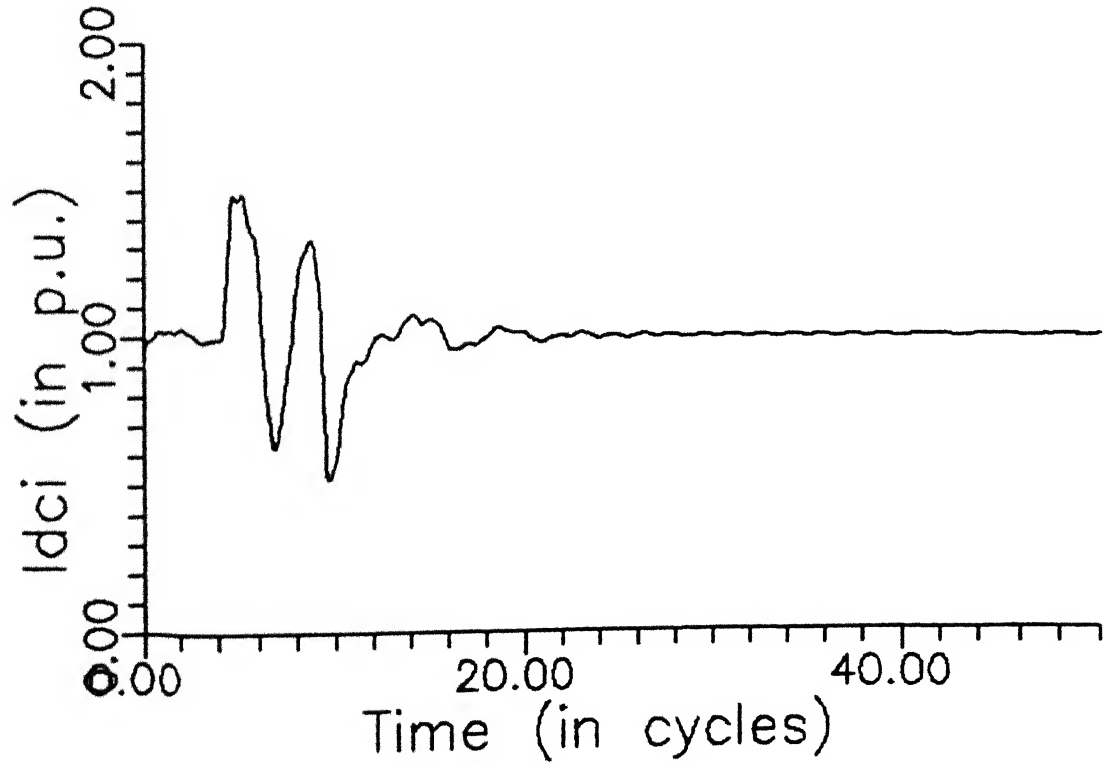


FIG. 4.66 INVERTER TERMINAL DC CURRENT FOR CASE 7

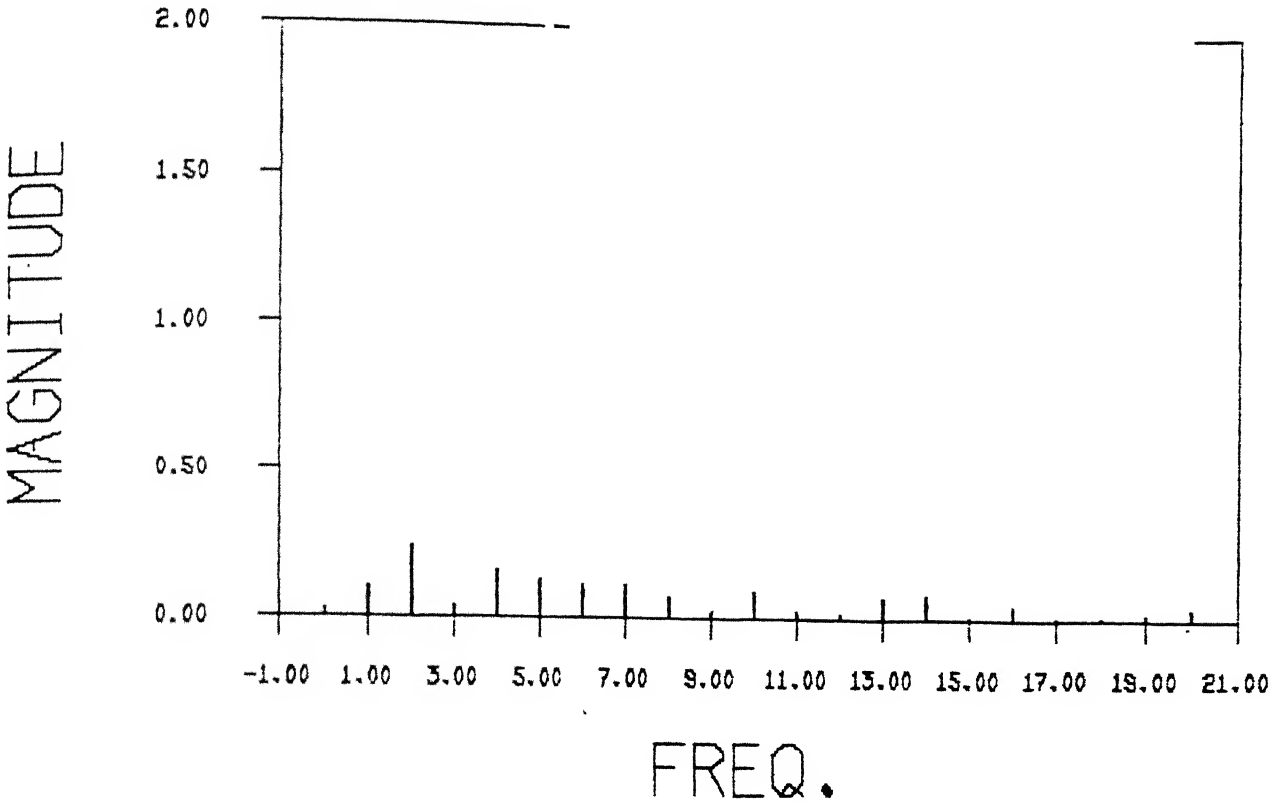


FIG. 4.67 HARMONIC COMPONENTS OF INVERTER AC VOLTAGE FOR CASE 7

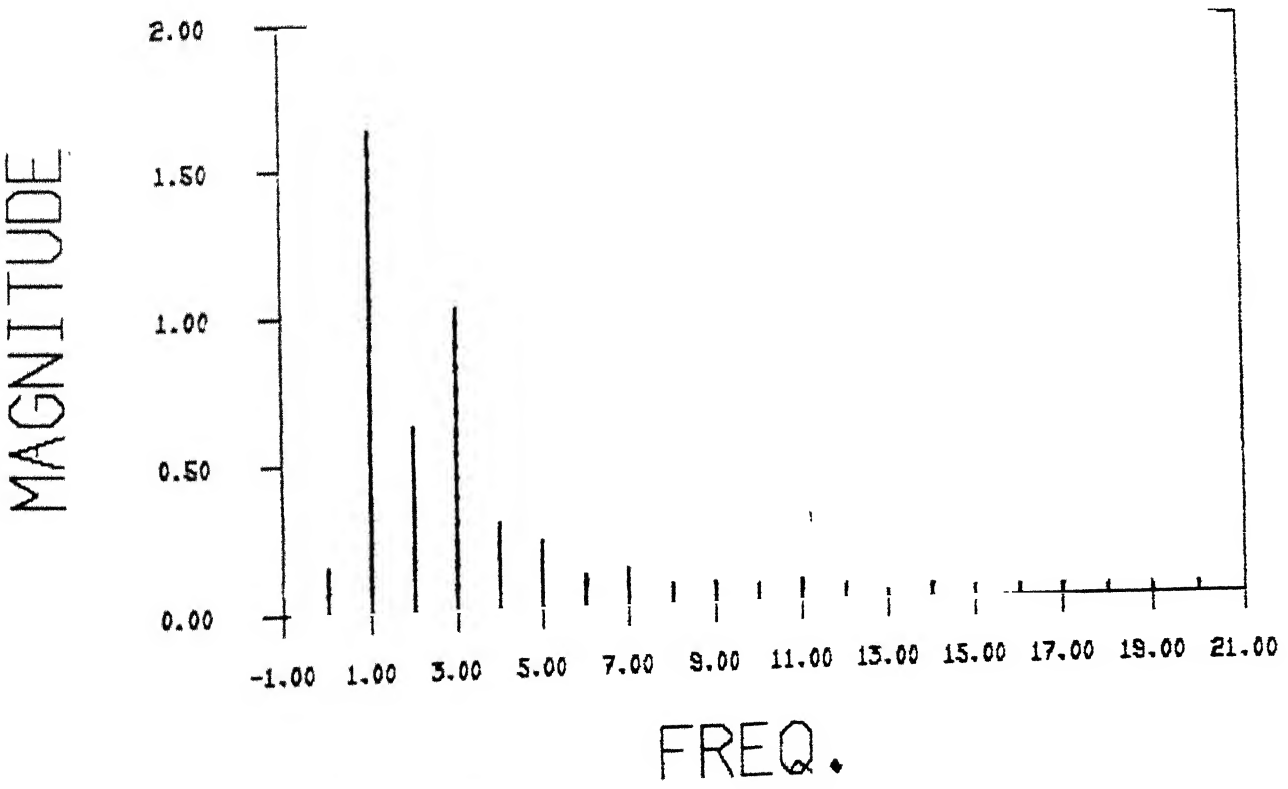


FIG. 4.68 HARMONIC COMPONENTS OF INVERTER AC CURRENT FOR CASE 7

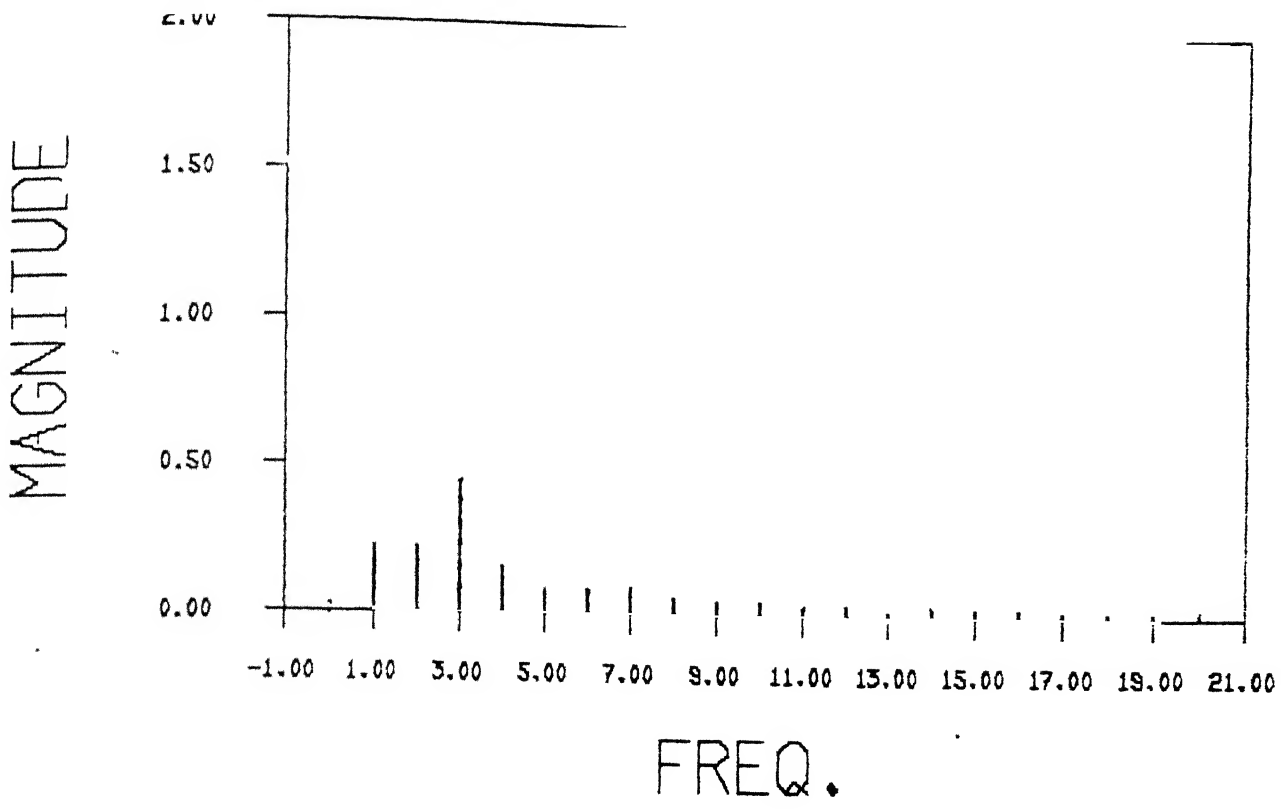


FIG. 4.69 HARMONIC COMPONENTS OF INVERTER DC VOLTAGE FOR CASE 7

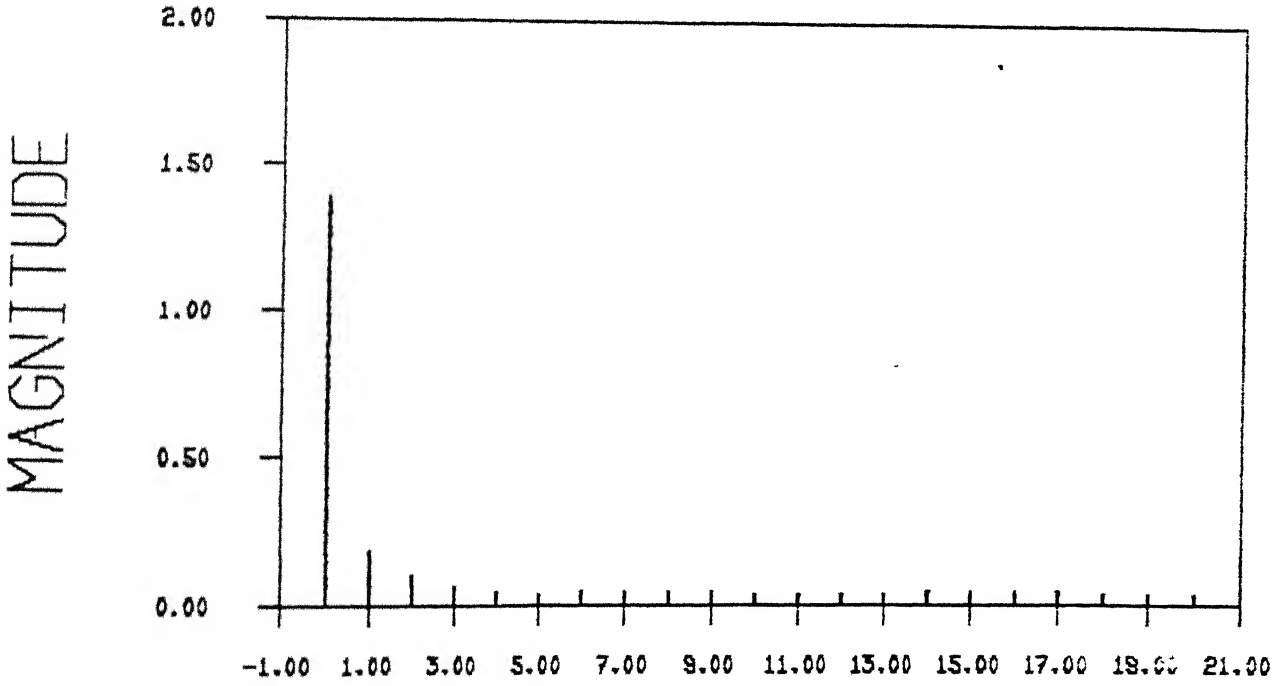


FIG. 4.70 HARMONIC COMPONENTS OF INVERTER DC CURRENT FOR CASE 7

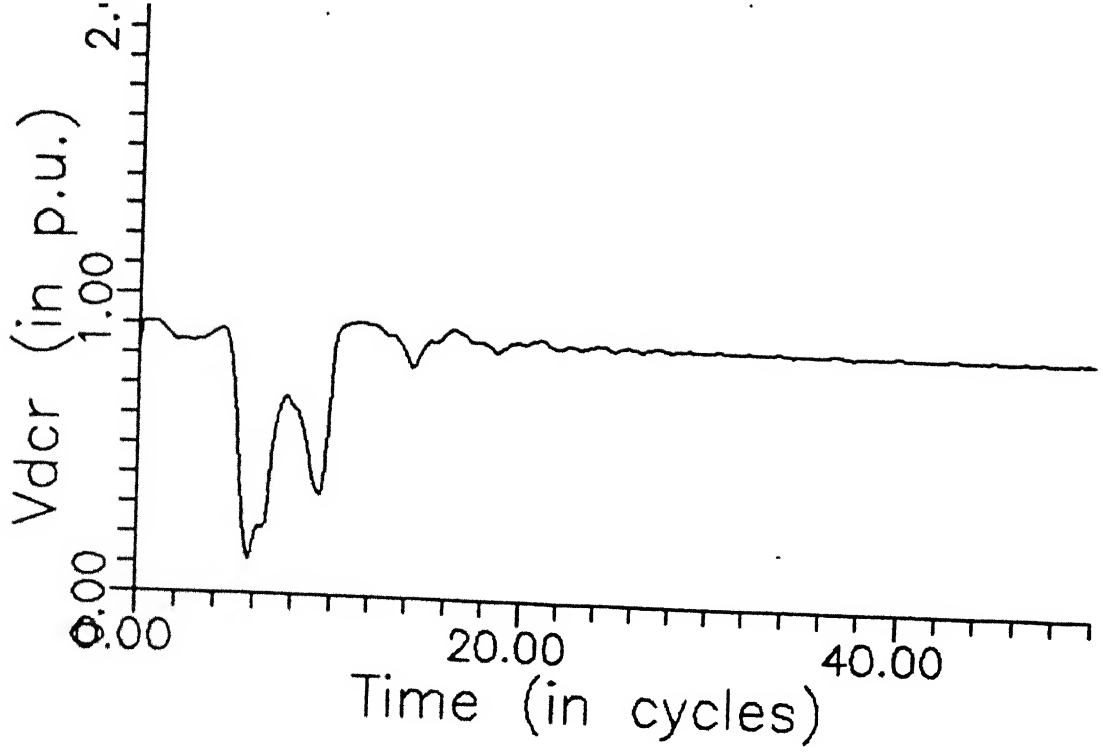


FIG. 4.71(a) RECTIFIER TERMINAL DC VOLTAGE FOR CASE 8

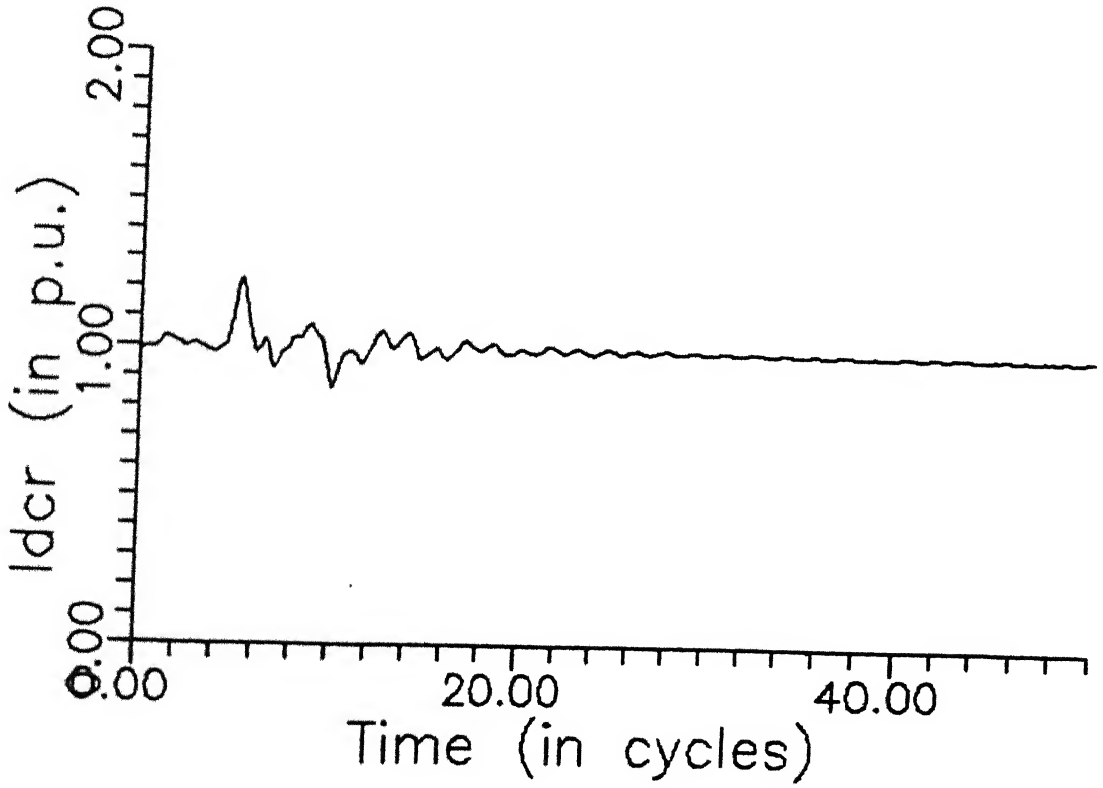


FIG. 4.71(b) RECTIFIER TERMINAL DC CURRENT FOR CASE 8

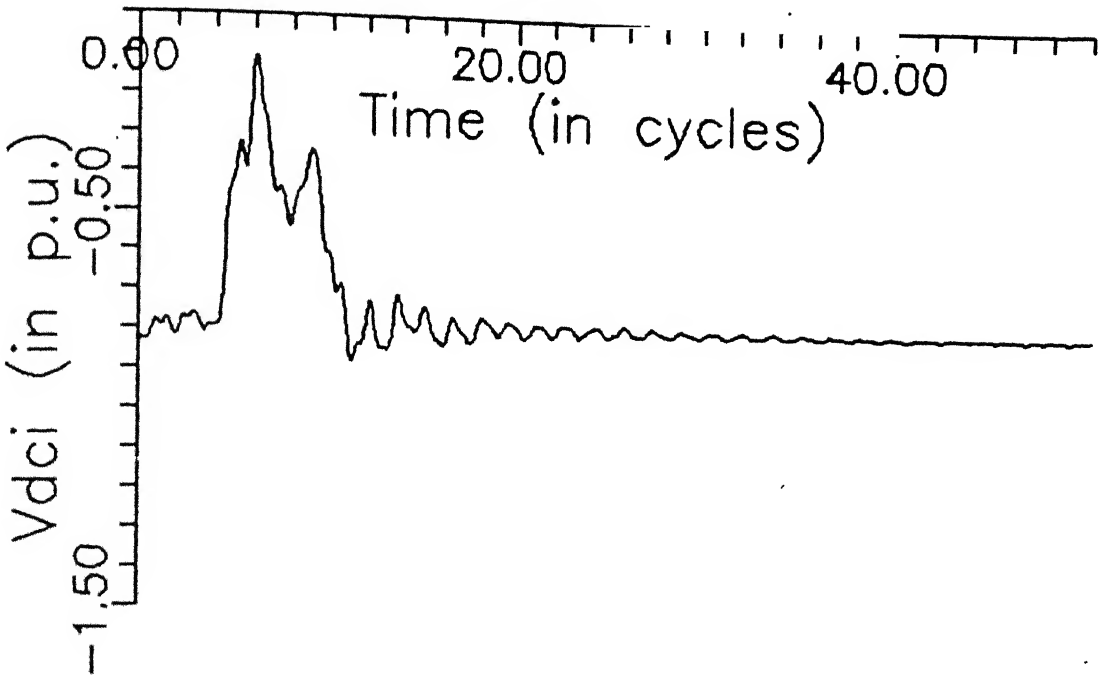


FIG. 4.72(a) INVERTER TERMINAL DC VOLTAGE FOR CASE 8

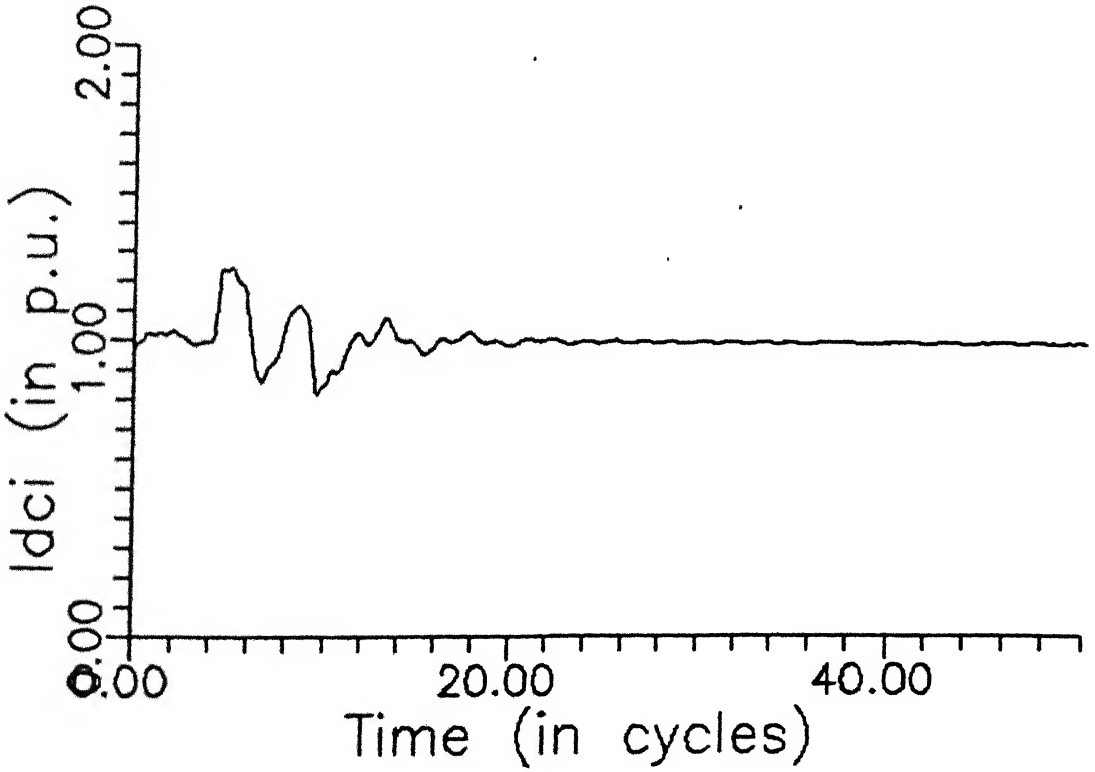


FIG. 4.72(b) INVERTER TERMINAL DC CURRENT FOR CASE 8

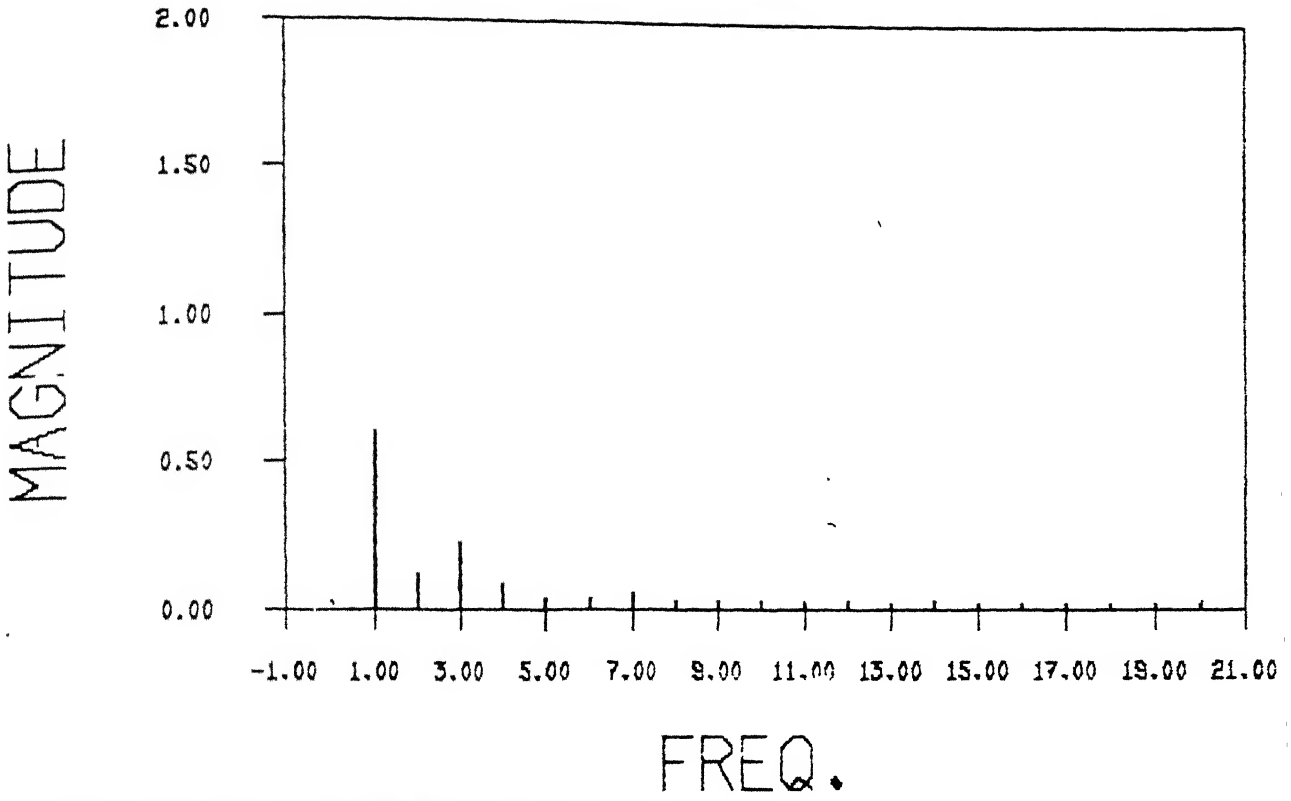


FIG. 4.73(a) HARMONIC COMPONENTS OF INVERTER AC VOLTAGE FO

CASE 8

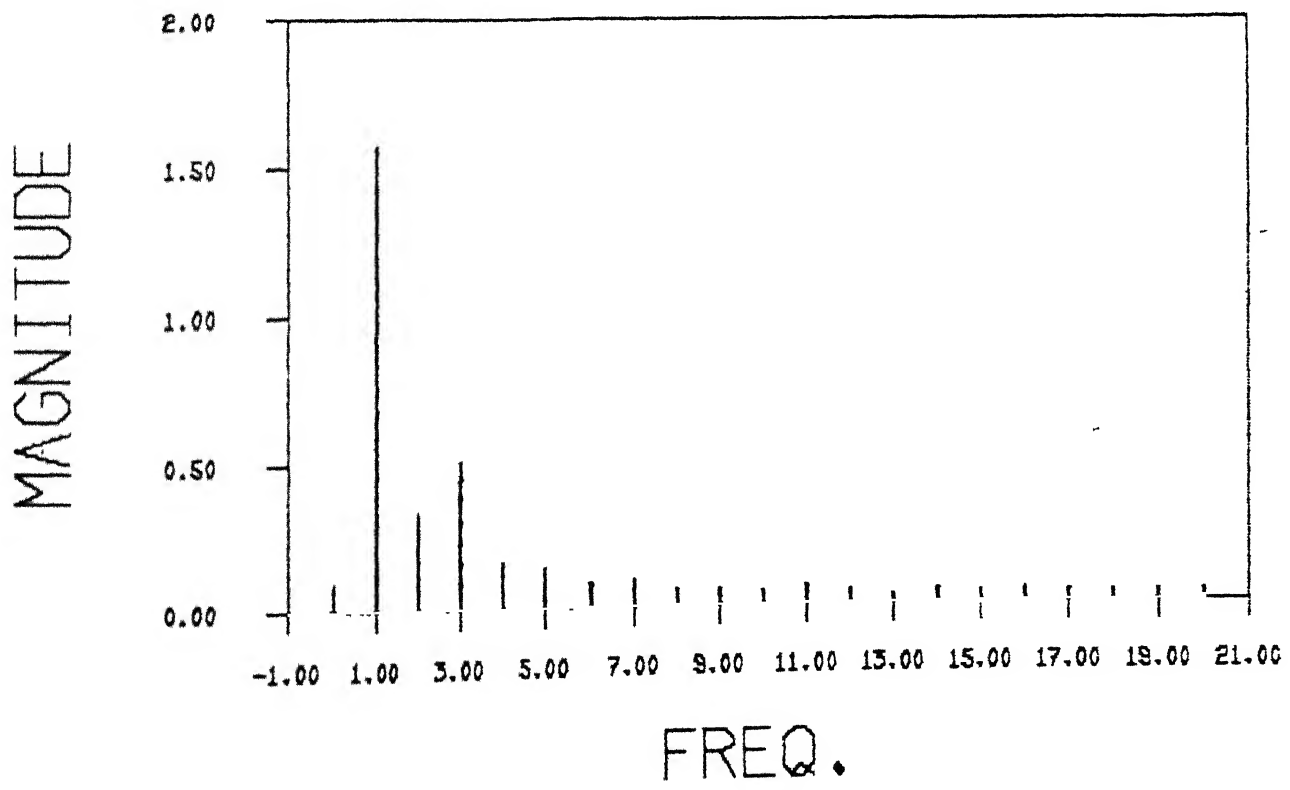


FIG. 4.73(b) HARMONIC COMPS. OF INVERTER AC CURRENT FOR CASE 8

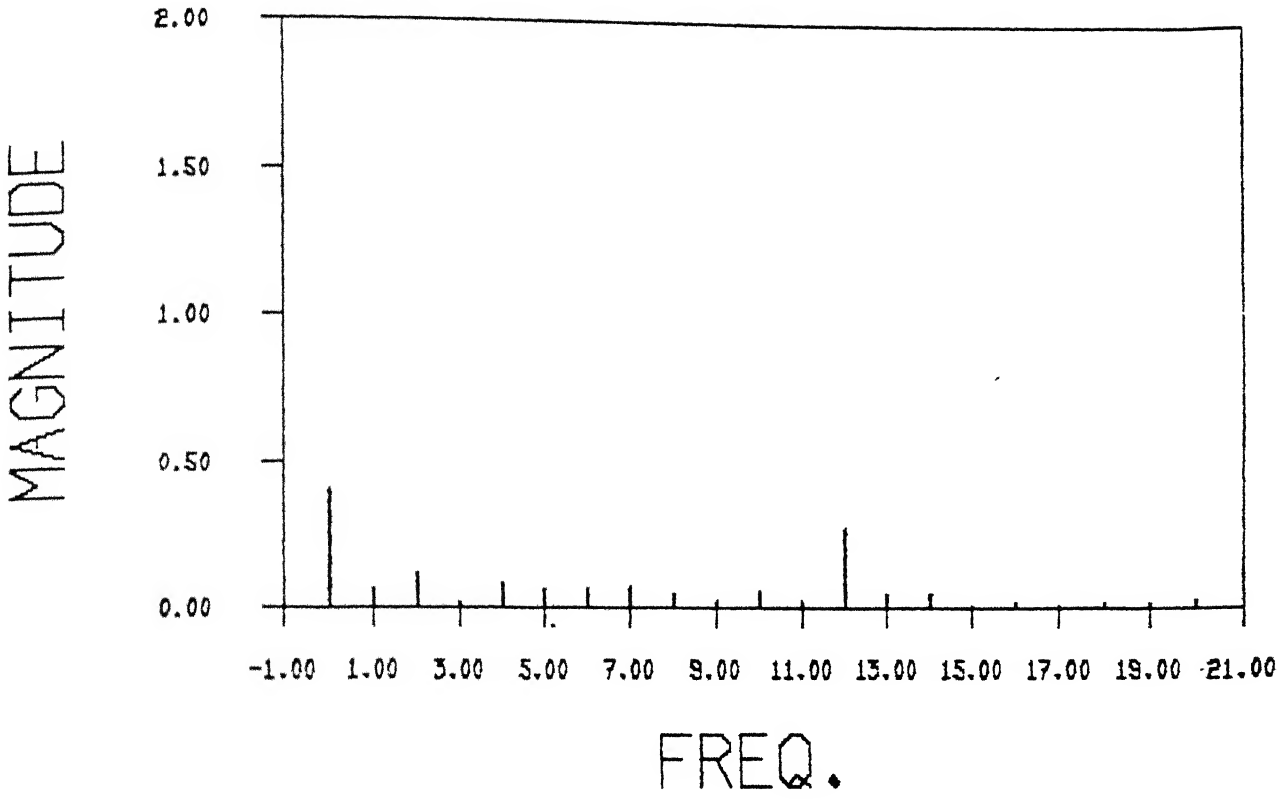


FIG. 4.74 (a) HARMONIC COMPS. OF INVERTER DC VOLTAGE FOR CASE 8

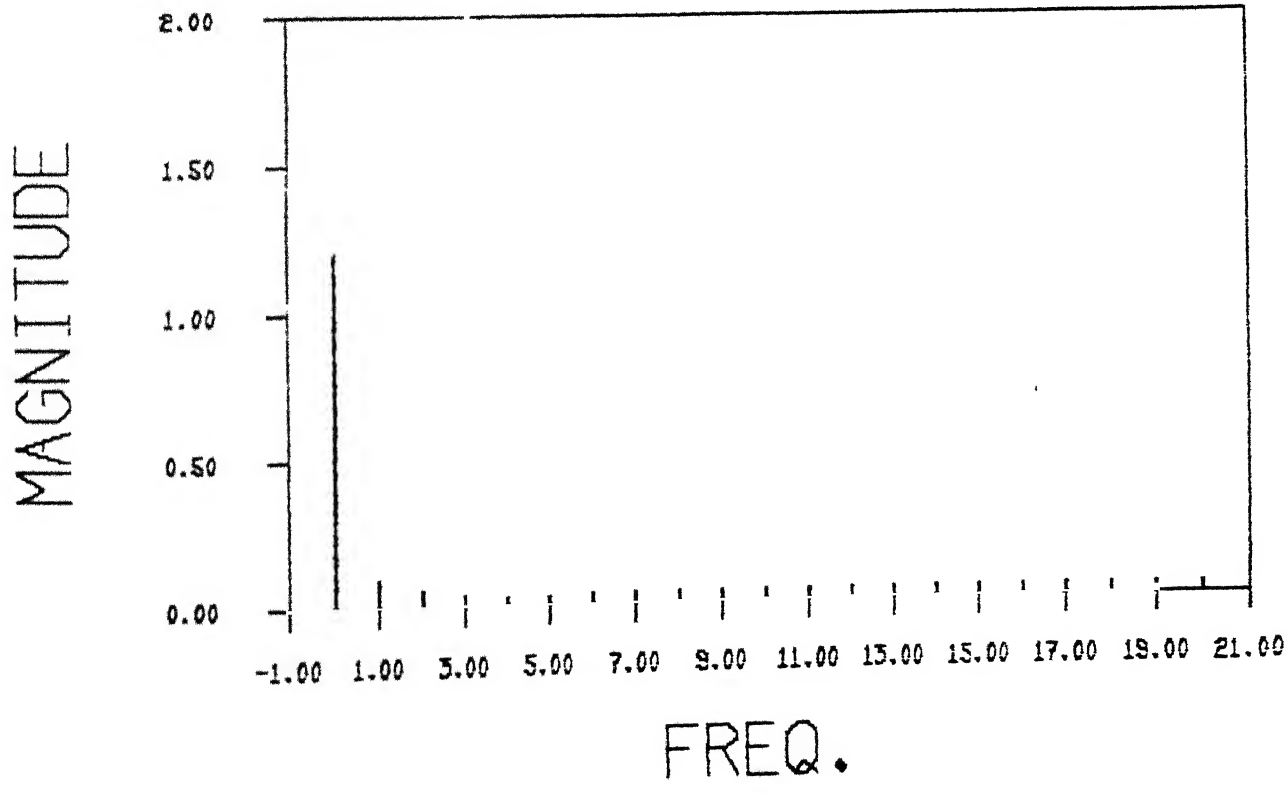
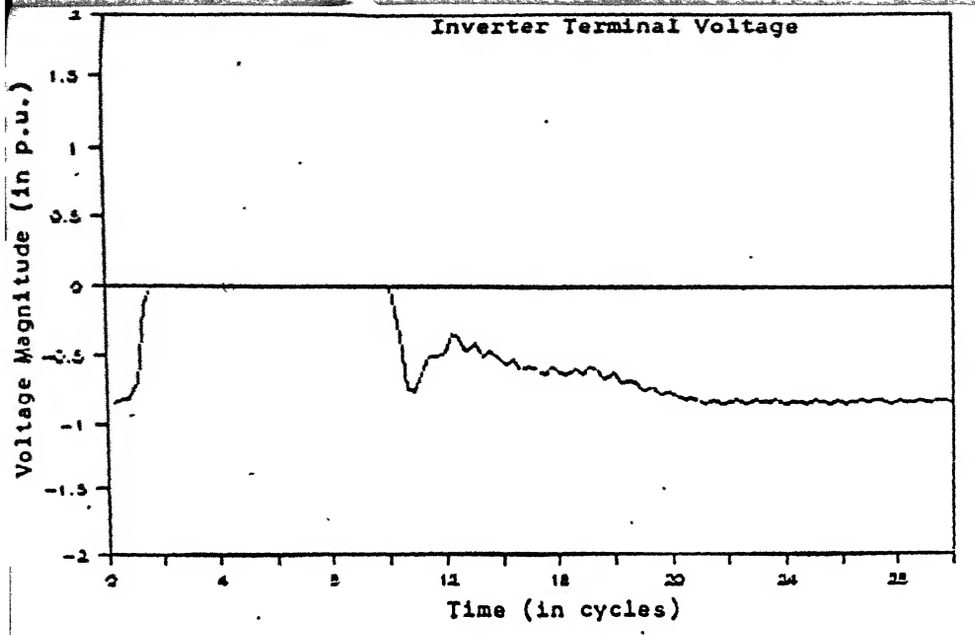
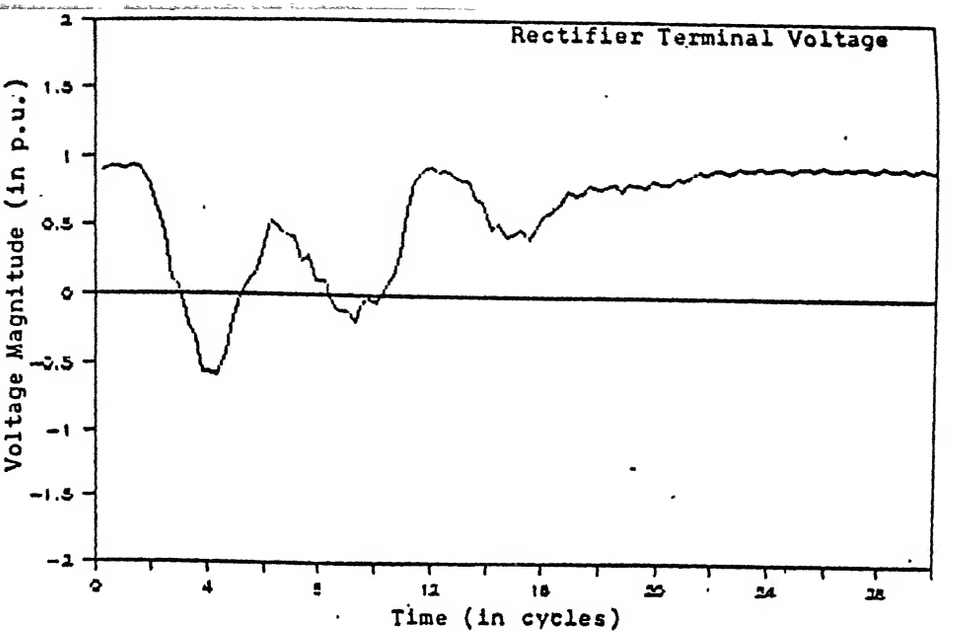
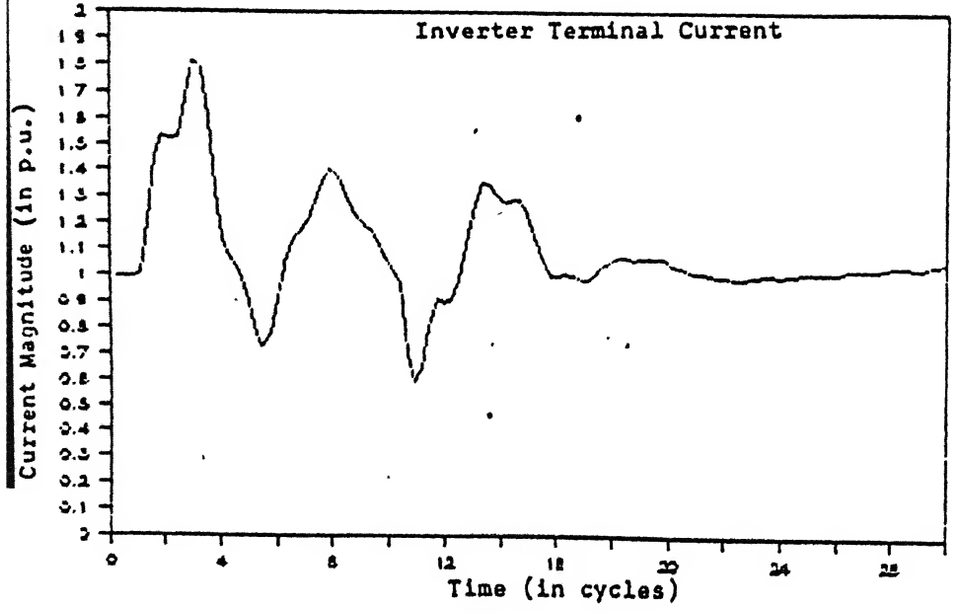


FIG. 4.74 (b) HARMONIC COMPS. OF INVERTER DC CURRENT FOR CASE 8







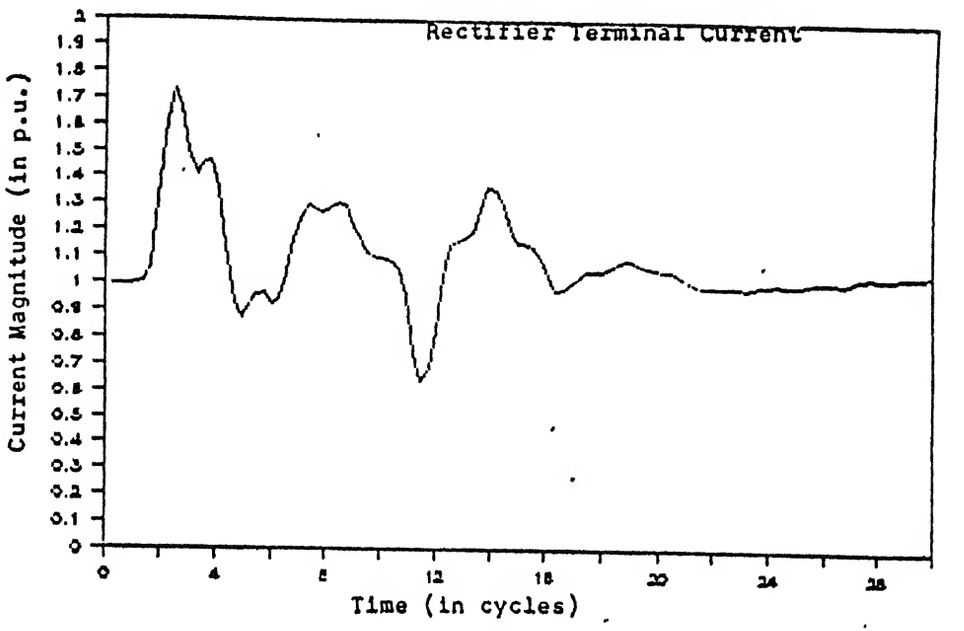
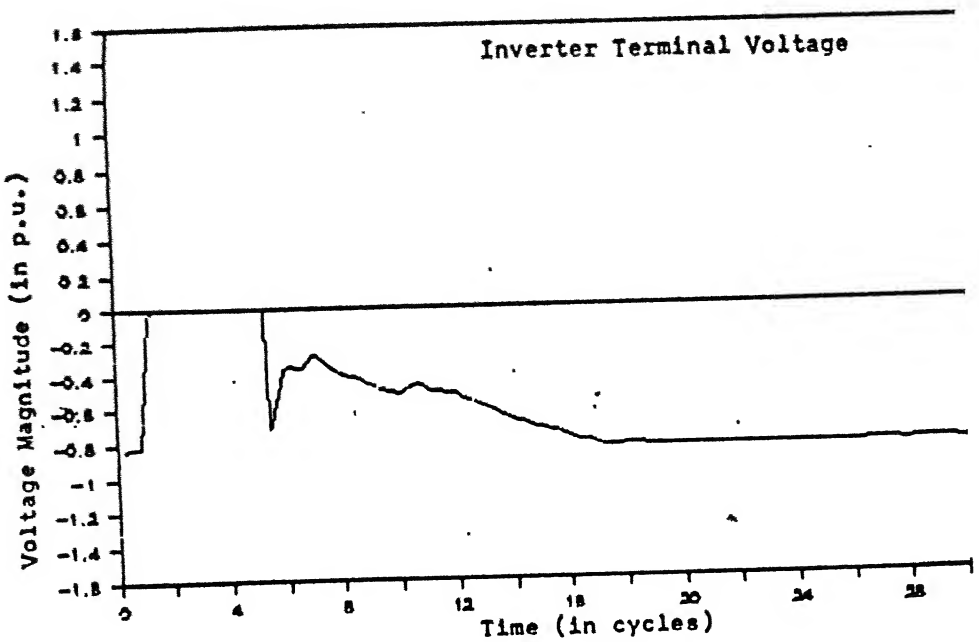
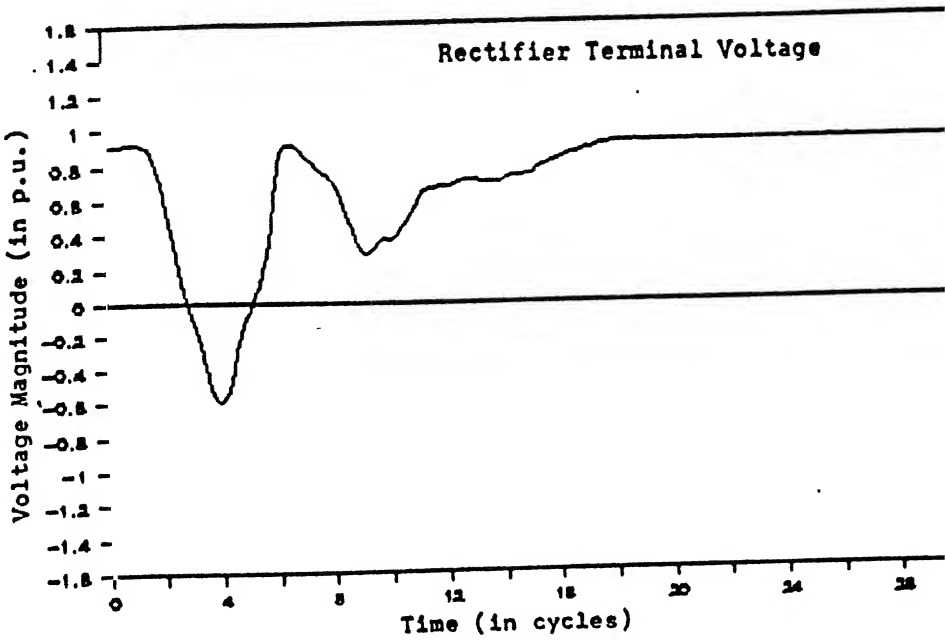
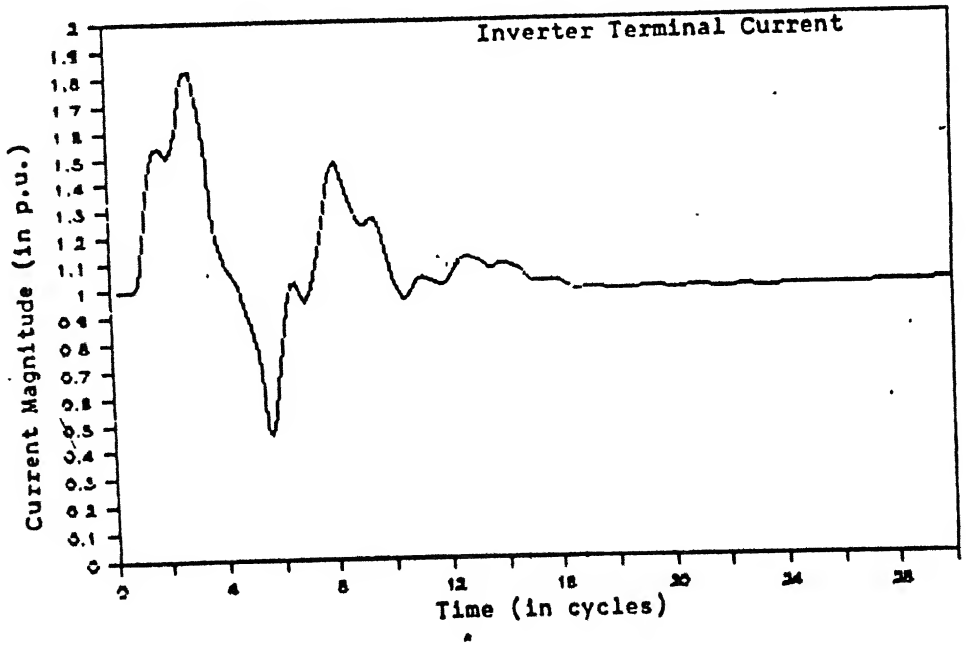


Fig. 4.75 99%, SINGLE PHASE, 10 CYCLE DIP AT INVERTER
NORMAL RECOVERY







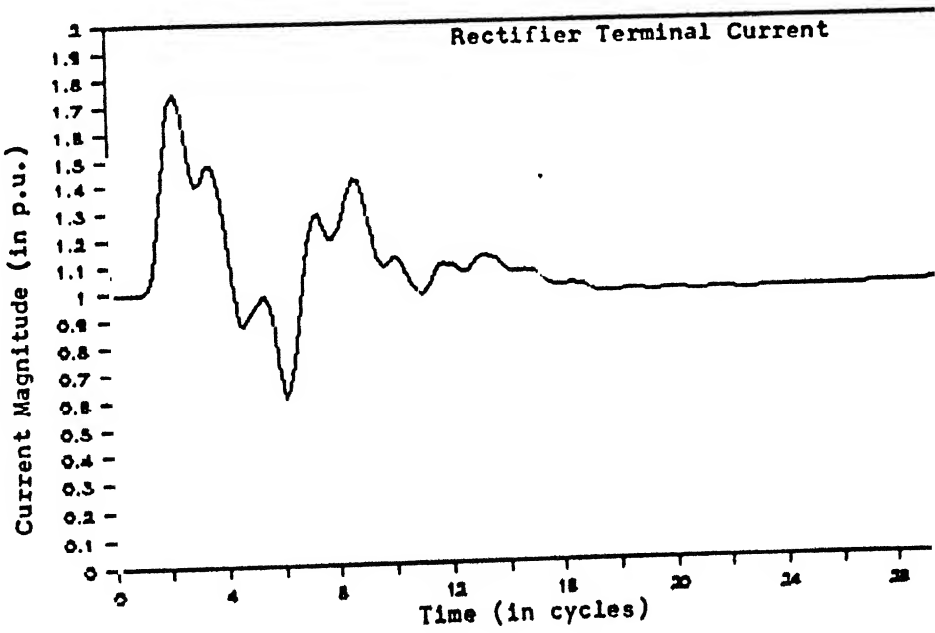
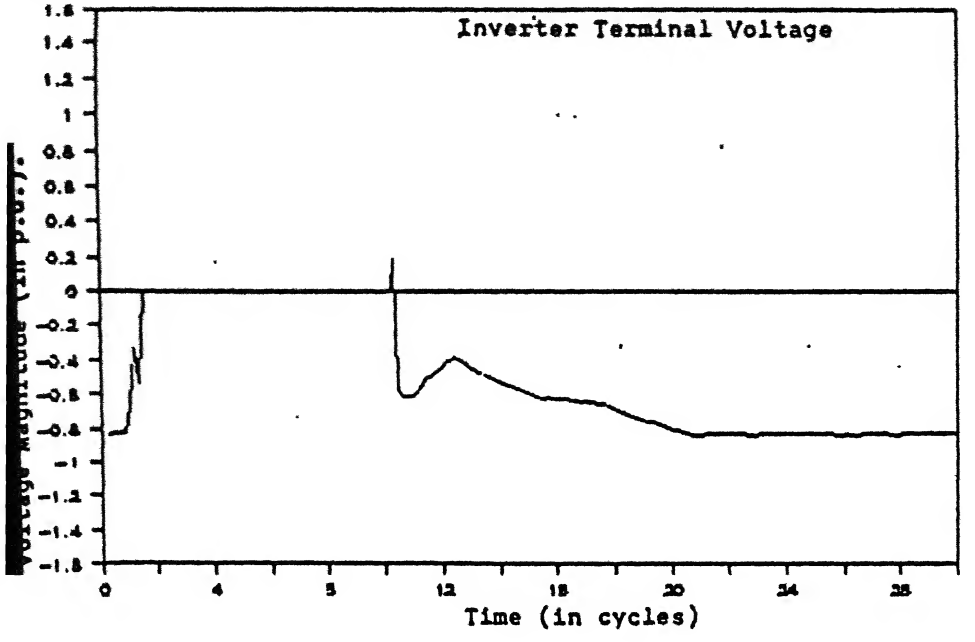
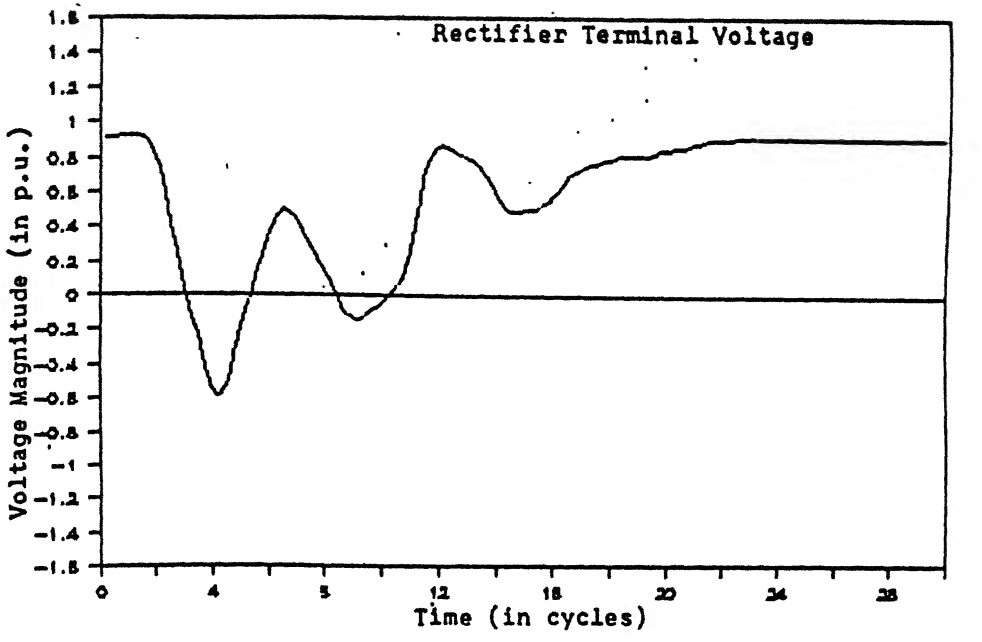
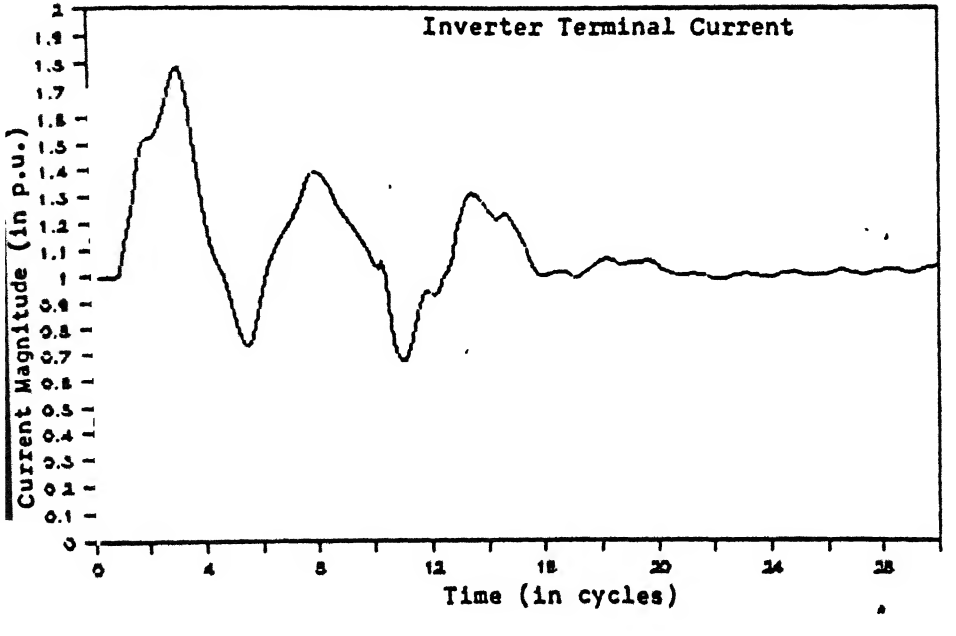


Fig. 4.76 99%, THREE PHASE, 4 CYCLE DIP AT INVERTER
NORMAL RECOVERY







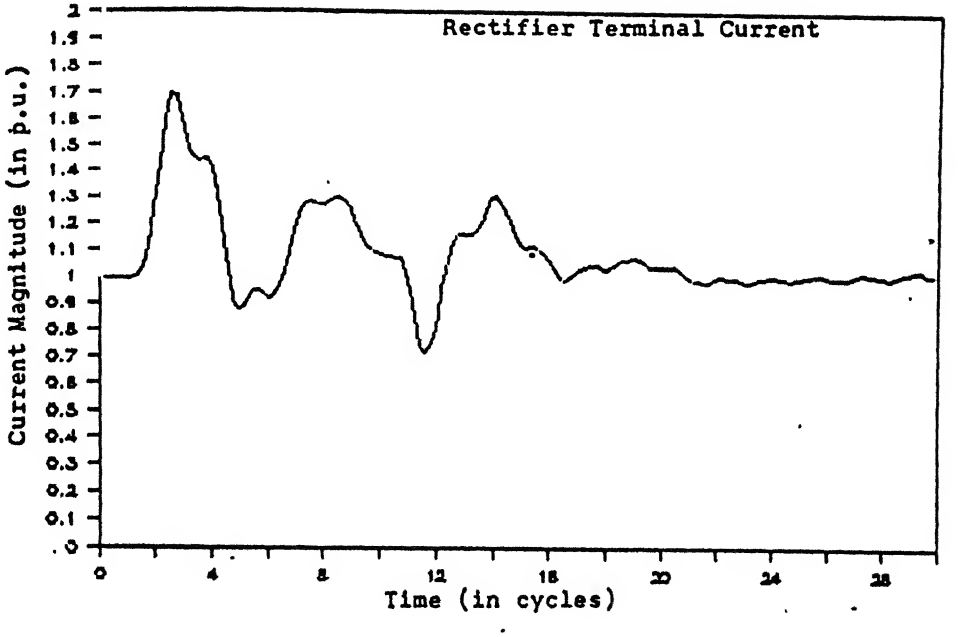


Fig. 4.77 50%, THREE PHASE, 10 CYCLE DIP AT INVERTER
NORMAL RECOVERY

Figures (4.75) to (4.77) are the system performance with thyristor inverter for case 5,7,8 respectively.

4.8 CONCLUSION

This chapter has been devoted to study the two terminal HVDC system performance with GTO inverter. A control strategy is made for GTO inverter to co-ordinate the conventional rectifier control. The optimization of control parameters has not been attempted. Both steady state and transient behaviour of the system without ac system representation have been studied. A comparision of the HVDC system with GTO inverter has been made with thyristor inverter.

CHAPTER 5

CONCLUSIONS AND FUTURE SCOPE OF WORK

This thesis has been mainly devoted to the development of a suitable model of the converter, consisting of six GTOs, for dynamic digital simulation. This model has been developed based on the graph theoretic approach which is conceptually simpler and leads to efficient formulation of the converter state equations corresponding to all possible modes of operation. The state equations are derived using network cutset matrix which can be modified conveniently depending upon converter conduction patterns. The investigation of performance of the GTO converter with active load has been made in both the modes of converter operation (rectification/inversion).

A major area of emphasis has been on the study of the performance of GTO inverter in HVDC link with appropriate inverter controls. The following conclusions have been drawn from above studies.

1. The lower order harmonics, which were present in the steady state operation of the converter with active load, are eliminated when GTO converter is used as inverter in HVDC link.

2. There is no requirement of reactive power at inverter end (i.e. power factor is maintained at unity).

3. The magnitudes of over-voltages due to fault are reduced

significantly with GTO inverter.

4. System recovers the steady state after clearing the fault without much disturbances within reasonable time.

5. The system performance is less affected to the rectifier faults than the inverter faults.

Since the major emphasis of this thesis is software developement to see the feasibility of GTO inverter in the HVDC system, the optimization of the controller parameters and the transient suppressor circuit parameters may lead to a further improvement in system performance. The following further additions can be made :

1. A suitable model can be developed using snubber circuit and also assuming that the switching devices are not ideal.

2. Other PWM schemes can be used to investigate the feasibility of GTO inverter in HVDC link.

3. The detailed representation of ac system can be included at both sides of the converter, so that performance of GTO inverter with weak ac system can be studied.

4. It may be thought to make leading power factor instead of unity power factor by suitable PWM schemes.

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APPENDIX I

Voltage drop occurs only P times for a half cycle of the current i_a consists of P pulses

$$E_x = \int_0^{t_1} L_s \frac{(di_b/dt).dt.2.P.3}{1/f}$$

$$= \int_0^{I_d} L_s.di_b.6.P.f$$

$$= L_s.I_d.6.P.f$$

$$=(3P/\pi).2.\pi f.L_s.I_d$$

$$E_x= (3P/\pi).\omega L_s.I_d \qquad (I.1)$$

Where t_1 is a time required for the current i_b to reach the value I_d . Average output voltage of converter,

$$E_d= E_0-E_x \qquad (I.2)$$

where E_0 is avearge output voltage when $L_s= 0.0$

E_0 can be calculated as follows :

$$E_0= (1/(\pi/3))\sum_{i=1}^{p} \int_{\pi/6+\alpha_i}^{\pi/6+\beta_i} E_{AB}\, d(\omega t) \qquad (I.3)$$

if $E_A = \sqrt{2}\, V_{ph}\, \text{Sin}\, (\omega t)$

$E_B = \sqrt{2}\, V_{ph}\, \text{Sin}\, (\omega t-2\pi/3)$

$E_C = \sqrt{2}\, V_{ph}\, \text{Sin}\, (\omega t-4\pi/3)$

then,

$E_{AB} =\sqrt{6}.V_{ph}.\text{Sin}\, (\omega t+\pi/6)$

$$E_0 = \frac{1}{\pi/3} \cdot \sqrt{6}.\ V_{ph} \cdot \sum_{i=1}^{p} \int_{\pi/6+\alpha_i}^{\pi/6+\beta_i} \mathrm{Sin}(\omega t+\theta_r)\ d(\omega t) \quad (I.4)$$

where $p=P/6$ and $\theta_r=\pi/6$

Solving and simplifying the equation (I.4),the following equation can be obtained :

$$E_0 = V_{do} \sum_{i=1}^{p} [\ \mathrm{Cos}\ (\pi/3+\alpha_i)-\mathrm{Cos}\ (\pi/3+\beta_i)] \quad (I.5)$$

where $V_{do} = \frac{3\sqrt{3}}{\pi}\sqrt{2}\ V_{ph}$

Voltage drop due to ac line resistance, inductance and switching devices is given below.

$$E_x = (\frac{3P}{\pi}\ \omega L_s + \lambda . R_s).I_d - V_T \quad (I.6)$$

where L_s and R_s are per phase source inductance and resistance respectively.

V_T= forward voltage of diodes*2 + 2* forward voltage of GTO

$$\lambda = \frac{\text{Total conduction period of succesive } \alpha_i \text{ and } \beta_i}{T}$$

$$T = 1/(2pf)$$

Hence average output voltage,

$$E_d = E_0 - \frac{(3P)}{\pi}.\omega L_s + \lambda R_s).\ I_d - V_T \quad (I.7)$$

APPENDIX II

The reduced incidence matrix of the graph given in chapter 3, taking node one as reference node is;

$[A]=$

	1	2	3	4	5	6	7	8	9	10	11	12
2	1	0	0	-1	0	0	0	0	1	1	0	-1
3	0	0	1	0	0	-1	-1	0	-1	-1	1	0
4	0	-1	0	0	1	0	1	0	0	0	-1	1
5	-1	0	-1	0	-1	0	0	1	0	0	0	0

The cut set matrices can be calculated by reduced incidence matrix [A] [21].

There are two mode of operations, one is power mode and other is freewheeling mode. Each mode have six cutset matrices. The twelve cutset matrices $[B_L^{ij}]$, each corresponding to the valve considered in the tree ,are given below. The superscript ij denotes the valve number , S_1 and S_2 taken in branch.

For power mode,

$[B_L^{61}]=$

	7	8	9	12	2	3	4	5
10	0	1	1	-1	0	-1	-1	-1
11	-1	0	0	-1	1	0	0	-1
6	0	-1	0	0	1	0	1	0
1	0	-1	0	0	0	1	0	1

$[B_L^{12}] =$

	7	8	9	12	3	4	5	6
10	0	1	1	-1	-1	-1	-1	0
11	-1	1	0	-1	0	-1	-1	-1
1	0	-1	0	0	1	0	1	0
2	0	-1	0	0	0	1	0	1

$[B_L^{23}] =$

	7	8	9	12	1	4	5	6
10	0	0	1	-1	1	-1	0	0
11	-1	1	0	-1	0	-1	-1	-1
2	0	-1	0	0	0	1	0	1
3	0	-1	0	0	1	0	1	0

$[B_L^{34}] =$

	7	8	9	12	1	2	5	6
10	0	-1	1	-1	1	1	0	1
11	-1	0	0	-1	0	1	-1	0
3	0	-1	0	0	1	0	1	0
4	0	-1	0	0	0	1	0	1

$[B_L^{45}] =$

	7	8	9	12	1	2	3	6
10	0	-1	1	-1	1	1	0	1
11	-1	-1	0	-1	1	1	1	0
4	0	-1	0	0	0	1	0	1
5	0	-1	0	0	1	0	1	0

$[B_L^{56}] =$

	7	8	9	12	1	2	3	4
10	0	0	1	-1	1	0	0	-1
11	-1	-1	0	-1	1	1	1	0
5	0	-1	0	0	1	0	1	0

6	0	−1	0	0	0	1	0	1

For free-wheeling mode,

$[B_L^{63}] =$

	7	8	9	12	1	2	4	5
10	0	0	1	−1	1	0	−1	0
11	−1	0	0	−1	0	1	0	−1
6	0	−1	0	0	0	1	1	0
3	0	−1	0	0	1	0	0	1

$[B_L^{14}] =$

	7	8	9	12	2	3	5	6
10	0	0	1	−1	1	−1	−1	1
11	−1	0	0	−1	1	0	−1	0
1	0	−1	0	0	0	1	1	0
4	0	−1	0	0	1	0	0	1

$[B_L^{25}] =$

	7	8	9	12	1	3	4	6
10	0	0	1	−1	1	0	−1	0
11	−1	0	0	−1	1	1	−1	−1
2	0	−1	0	0	0	0	1	1
5	0	−1	0	0	1	1	0	0

All the other mode are $[B_L^{36}]$, $[B_L^{41}]$, and $[B_L^{52}]$. They are same as matrices $[B_L^{63}]$,$[B_L^{14}]$ and $[B_L^{25}]$ respectively . Only defferrence is interchange of last two rows.

APPENDIX III

Putting the value of $\underline{V}_{L1}$ from equation (3.18) into equation (3.14), following equation can be obtained :

$$[B_{L11}]^T . \underline{V}_{B1} = \left[[R_a]+\omega[L_a]p\right] \underline{i}_{L1} + \underline{e}$$

Above equation can be rearranged as

$$p\,\underline{i}_{L1} = -[\omega L_a]^{-1}\underline{i}_{L1} + [\omega L_a]^{-1}[B_{L11}]^T \underline{V}_{B1} - [\omega\ L]^{-1}\underline{e}$$

or,

$$p\,\underline{i}_{L1} = [K_1]\underline{i}_{L1} + [K_2]\underline{V}_{B1} + [K_3]\underline{e} \qquad \text{(III.1)}$$

where $[K_1] = -[\omega L_a]^{-1}[R_a]$

$[K_2] = [\omega L_a]^{-1}[B_{L11}]^T$

$[K_3] = -[\omega L_a]^{-1}$

Premultiply $[B_{L14}]^T$ in equation (3.24) and equating with equation (3.21),

$$[B_{L14}]^T p\underline{V}_{B1} = [B_{L14}]^T[R_f]p\underline{i}_{B1} + [B_{L14}]^T[C'_f]\underline{i}_{B1}$$

or,

$$[0] = [B_{L14}]^T[R_f]p\underline{i}_{B1} + [B_{L14}]^T[C'_f]\underline{i}_{B1}$$

Putting the value of $\underline{i}_{B1}$ in above equation from equation (3.16),

$$[0] = [B_{L14}]^T[R_f]p\left[-[B_{L11}]\underline{i}_{L1} - [B_{L12}]\underline{i}_{L2} - [B_{L14}]\underline{i}_{L4}\right] +$$

$$[B_{L14}]^T[C'_f]\left[-[B_{L11}]\underline{i}_{L1} - [B_{L12}]\underline{i}_{L2} - [B_{L14}]\underline{i}_{L4}\right] \qquad \text{(III.2)}$$

Premultiply $[B_{L12}]^T$ in equation (3.24) and equating with equation (3.19), this can be obtained:

$$[B_{L12}]^T \underline{pV}_{B1} = [B_{L12}]^T [R_f] \underline{pi}_{B1} + [B_{L12}]^T [C'_f] \underline{i}_{B1}$$

and

$$p[B_{L12}]^T \underline{V}_{B1} = \underline{pV}_{L2}$$

$$\rightarrow \quad \underline{pV}_{L2} = [B_{L12}]^T [R_f] \underline{pi}_{B1} + [B_{L12}]^T [C'_f] \underline{i}_{B1}$$

Comparing above equation to equation (3.25)

$$R.\underline{pi}_{L2} + C_f.\underline{i}_{L2} = [B_{L12}]^T [R_f] \underline{pi}_{B1} + [B_{L12}]^T [C'_f] \underline{i}_{B1}$$

$$= [B_{L12}]^T [R_f] p\left[-[B_{L11}]\underline{i}_{L1} - [B_{L12}]\underline{i}_{L2} - [B_{L14}]\underline{i}_{L4}\right] + [B_{L12}]^T [C'_f]\left[-[B_{L11}]\underline{i}_{L1} - [B_{L12}]\underline{i}_{L2} + [B_{L14}]\underline{i}_{L4}\right]$$

Rearranging above equation, the following equation ca be abtained:

$$\left[R + [B_{L12}]^T [R_f] [B_{L12}]\right] \underline{pi}_{L2} = -\left[C_f + [B_{L12}]^T [C'_f] [B_{L12}]\right] \underline{i}_{L2} - [B_{L12}]^T [R_f] [B_{L12}] \underline{pi}_{L1} - [B_{L12}]^T [R_f] [B_{L14}] \underline{i}_{L4} - [B_{L12}]^T [C'_f] [B_{L12}] \underline{i}_{L1} - [B_{L12}]^T [C'_f] [B_{L14}] \underline{i}_{L4}$$

The above equation can be simplified as,

$$\underline{pi}_{L2} = -[K_4]\underline{i}_{L2} + [K_5]\underline{pi}_{L1} + [K_6]\underline{pi}_{L4} + [K_7]\underline{i}_{L1} + [K_8]\underline{i}_{L4} \qquad \text{(III.3)}$$

where,

$$[K_4] = -C_f/R \text{ (always)}$$

$$[K_5] = -(1/3R).[B_{L12}]^T [R_f] [B_{L11}]$$

$$[K_6] = -(1/3R).[B_{L12}]^T [R_f] [B_{L14}]$$

$$[K_7] = -(1/3R).[B_{L12}]^T [C'_f] [B_{L11}]$$

$$[K_8] = -(1/3R).[B_{L12}]^T [C'_f] [B_{L14}]$$

Equation (III.2) can be further simplified as follows:

$$[O]=[B_{L14}]^T[B_{L11}]R\ \underline{pi}_{L1}+[B_{L14}]^T[B_{L11}][C_f]\underline{i}_{L1}+[B_{L14}]^T[R_f][B_{L12}]$$

$$\underline{pi}_{L2}+[B_{L14}]^T[B_{L12}]C_f.\underline{i}_{L2}+[B_{L14}]^T[B_{L14}][R_f]\underline{pi}_{L4}+$$

$$[B_{L14}]^T[C'_f][B_{L14}]\underline{i}_{L4}$$

If the values of resistances and capacitances of transient suppresor circuit of each phase are equal, then the matrices $[R_f]$ and $[C'_f]$ are unity matrix with a multification of a constant.

Simplifying the above equation and putting the value of $[pi_{L2}+(C_f/R).i_{L2}]$ from equation (III.3).

$$[O]=\left[[B_{L14}]^T[B_{L12}][K_5]R+[B_{L14}]^T[R_f][B_{L11}]\right]\underline{pi}_{L1}+$$

$$\left[[B_{L14}]^T[B_{L12}][K_6]R+[B_{L14}]^T[R_f][B_{L14}]\right]\underline{pi}_{L4}+$$

$$\left[[B_{L14}]^T[B_{L12}][K_7]R+[B_{L14}]^T[C'_f][B_{L11}]\right]\underline{i}_{L1}+$$

$$\left[[B_{L14}]^T[B_{L12}][K_8]R+[B_{L14}]^T[C'_f][B_{L14}]\right]\underline{i}_{L4}$$

Above equation can be simplified by using equation (III.1)

$$\underline{pi}_{L1}=[K_{11}]\underline{i}_{L4}+[K_{12}]\underline{i}_{L1}+[K_{13}]\underline{V}_{B1}+[K_{14}]\underline{e} \qquad (IV.4)$$

Where,

$$[K'_8]=[B_{L14}]^T[B_{L12}][K_6]R+[B_{L14}]^T[R_f][B_{L14}]$$

$$[K_{10}]=[B_{L14}]^T[B_{L12}][K_7]R+[B_{L14}]^T[C'_f][B_{L11}]$$

$$[K_{11}]=-[K'_8]^{-1}\left[[B_{L14}]^T[B_{L12}][K_8]R+[B_{L14}]^T[C'_f][B_{L14}]\right]$$

$$[K_{12}]=-[K_8]^{-1}\left[[B_{L14}]^T[B_{L12}][K_5]R+[B_{L14}]^T[R_f][B_{L14}]\right][K_1]+[K_{10}]$$

$$[K_{13}]=-[K_8]^{-1}\left[[B_{L14}]^T[B_{L12}][K_5]R+[B_{L14}]^T[R_f][B_{L11}]\right][K_2]$$

$$[K_{14}]=-[K'_8]^{-1}\left[[B_{L14}]^T[B_{L12}][K_5]R+[B_{L14}]^T[R_f][B_{L11}]\right][K_3]$$

From equation (3.24),

$$\underline{pV}_{B1}=[R_f][\underline{pi}_{B1}+[C'_f][\underline{i}_{B1}$$

$$=\Big[[R_f][B_{L11}][\underline{pi}_{L1}+[R_f][B_{L12}][\underline{pi}_{L2}+[R_f][B_{L14}][\underline{pi}_{L4}+[C'_f][B_{L11}][\underline{i}_{L1}$$

$$+[C'_f][B_{L12}][\underline{i}_{L2}+[C'_f][B_{L14}][\underline{i}_{L4}$$

$$=[R_f][B_{L11}][\underline{pi}_{L1}+[B_{L12}]R[\underline{pi}_{L2}+(C_f/R)\underline{i}_{L2}]+[R_f][B_{L14}][\underline{pi}_{L4}+$$

$$[C'_f][B_{L11}][\underline{i}_{L1}+[C'_f][B_{L14}][\underline{i}_{L4}$$

Putting the value of $[\underline{pi}_{L2}+(C_f/R)\underline{i}_{L2}]$ from equation (III.3)

$$\underline{pV}_{B1}=-\Big[\Big([R_f][B_{L11}][\underline{pi}_{L1}+[B_{L12}]R\Big[[K_5][\underline{pi}_{L1}+[K_6][\underline{pi}_{L4}+[K_7][\underline{i}_{L1}+$$

$$[K_8][\underline{i}_{L4}+\Big]+[R_f][B_{L14}][\underline{pi}_{L4}+[C'_f][B_{L11}][\underline{i}_{L1}+[C'_f][B_{L14}][\underline{i}_{L4}\Big)\Big]$$

$$=-\Big[[R_f][B_{L11}]+[B_{L12}][K_5]R\Big]\underline{pi}_{L1}-\Big[[R_f][B_{L14}]+[B_{L12}][K_6]R\Big]\underline{pi}_{L4}-$$

$$\Big[[B_{L12}][K_7]R+[C'_f][B_{L11}]\Big]\underline{i}_{L1}-\Big[[B_{L12}][K_8]R+[C'_f][B_{L14}]\Big]\underline{i}_{L4}$$

=>

$$\underline{pV}_{B1}=-\Big[[K_{19}][\underline{pi}_{L1}+[K_{20}]\underline{Pi}_{L4}+[K_{21}][\underline{i}_{L1}+[K_{22}][\underline{i}_{L4}\Big] \qquad \text{(III.5)}$$

Where,

$$[K_{19}]=[R_f][B_{L11}]+[B_{L12}][K_5]R$$

$$[K_{20}]=[R_f][B_{L14}]+[B_{L12}][K_6]R$$

$$[K_{21}]=[B_{L12}][K_7]R+[C'_f][B_{L11}]$$

$$[K_{22}]=[B_{L12}][K_8]R+[C'_f][B_{L14}]$$

Using equation (III.1) and (III.4),the equation can be simplified as follows:

$$p\underline{V}_{B1}=-\left[\left([K_{19}][K_1]+[K_{20}][K_{12}]+[K_{21}]\right)\underline{i}_{L1}+\left([K_{20}][K_{11}]+[K_{22}]\right)\underline{i}_{L4}\right.$$
$$\left.+\left([K_{19}][K_2]+[K_{20}][K_{13}]\right)\underline{V}_{B1}+\left([K_{19}][K_3]+[K_{20}][K_{14}]\right)\underline{e}\right]$$

or,

$$p\underline{V}_{B1}=-[K_{15}]\underline{i}_{L1}-[K_{16}]\underline{i}_{L4}-[K_{17}]\underline{V}_{B1}-[K_{18}]\underline{e} \qquad \text{(III.6)}$$

Where,

$$[K_{15}]=[K_{19}][K_1]+[K_{20}][K_{12}]+[K_{21}]$$
$$[K_{16}]=[K_{20}][K_{11}]+[K_{22}]$$
$$[K_{17}]=[K_{19}][K_2]+[K_{20}][K_{13}]$$
$$[K_{18}]=[K_{19}][K_3]+[K_{20}][K_{14}]$$

APPENDIX IV

The datas of source, converter and dc load for digital simulation of the GTO converter are given below :

(a) AC source data

(i) Ac system frequency = 50 Hz

(ii) Source voltage = 94.11 Volts line to ground

(iii) Source resistance = 0.158 ohms per phase

(iv) Source inductance = 0.073 mH per phase

(b) Converter data

(i) Overvoltage suppresion circuit elements

Resistance = 6 ohms

Inductance = 8 μF

(ii) Number of pulses per cycle (P) = 12

(iii) Modulation index for EPWM = 0.8

(c) Load data

(i) Smoothing resistance (Rd) = 3.1 ohms

(ii) smoothing inductance (Ld) = 24.0 mH

(iii) Back emf (Vc) = 160.0 volts

These datas are for rectifier operation . For inverter operation all other datas are same except back emf which is taken as −180.0 volts.

APPENDIX V

MODE SEQUENCE OF RECTIFIER OPERATION FOR m=0.8 AND P= 12

G_1	G_2	G_3	G_4	G_5	G_6	INTERVAL	PERIOD IN DEG.
X					X	$\alpha_1 - \beta_1$	24*
X			X			$\beta_1 - \alpha_2$	6**
X					X	$\alpha_2 - \beta_2$	24
X			X			$\beta_2 - \alpha_3$	6
X	X					$\alpha_3 - \beta_3$	24
	X			X		$\beta_3 - \alpha_4$	6
X	X					$\alpha_4 - \beta_4$	24
	X			X		$\beta_4 - \alpha_5$	6
	X	X				$\alpha_5 - \beta_5$	24
		X			X	$\beta_5 - \alpha_6$	6
	X	X				$\alpha_6 - \beta_6$	24
		X			X	$\beta_6 - \alpha_7$	6
		X	X			$\alpha_7 - \beta_7$	24
X			X			$\beta_7 - \alpha_8$	6
		X	X			$\alpha_8 - \beta_8$	24
X			X			$\beta_8 - \alpha_9$	6
			X	X		$\alpha_9 - \beta_9$	24
	X			X		$\beta_9 - \alpha_{10}$	6

G_1	G_2	G_3	G_4	G_5	G_6	INTERVAL	PERIOD IN DEG.
			X	X		$\alpha_{10} - \beta_{10}$	24
	X			X		$\beta_{10} - \alpha_{11}$	6
				X	X	$\alpha_{11} - \beta_{11}$	24
		X			X	$\beta_{11} - \alpha_{12}$	6
				X	X	$\alpha_{12} - \beta_{12}$	24
		X			X	$\beta_{12} - \alpha_{13}$	6
X					X	$\alpha_1 - \beta_1$	24

* 24^0 degree indicates the power mode of converter

** 6^0 degree indicates the free wheeling mode.

X shows the GTOs conduction for a given period.

They are related by following equation :

$$\frac{2*\pi}{P} = \text{POWER MODE} + \text{FREE WHEELING MODE}$$

APPENDIX VI

SYSTEM DATA (adapted from reference [14])

DC base voltage = 100 kV

DC base current = 1 kA

DC base impedance = 100 Ohms

Rated Power of DC Link = 240 MW for 12 pulse system

= 120 MW for 6 pulse system

AC system frequency = 50 Hz

Bridge Transformer:

Resistance $R_{c1} = R_{c2} = 0.5$ Ohms

Commutating Reactance $X_{c1} = X_{c2} = 6.283$ Ohms

Smoothing Reactor:

Resistance $R_{d1} = R_{d2} = 0.1$ Ohms

Reactance $X_{d1} = X_{d2} = 314.159$ Ohms

Transmission Line:

Total resistance = 8.64 Ohms

Total inductance = 0.50148 H

Total capacitance = 54.1645 μF

Any number of PI sections upto a maximum of 10 may be specified

Digital Controller (adapted from reference [20])

a) Constant Current Controller

$K_1 = 0.9$ radians/per unit current

$K_2 = 0.1$ radians^2/per unit current

b) INVERTER CONSTANT CURRENT CONTROLLER

$K_1 = 0.8$; P=12

$T_1 = 0.025$; CONSTANT m = 0.8

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